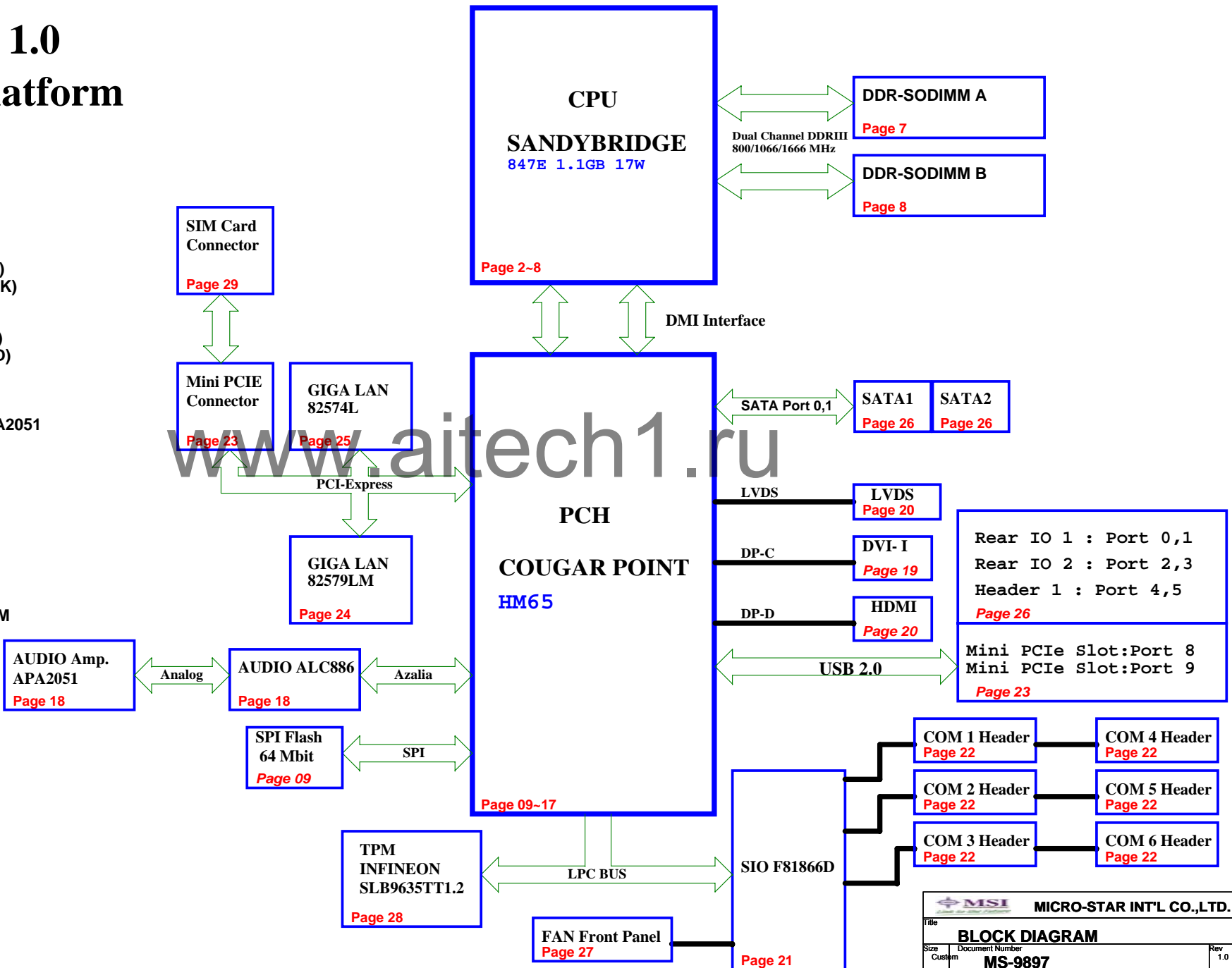


# Huron River Platform

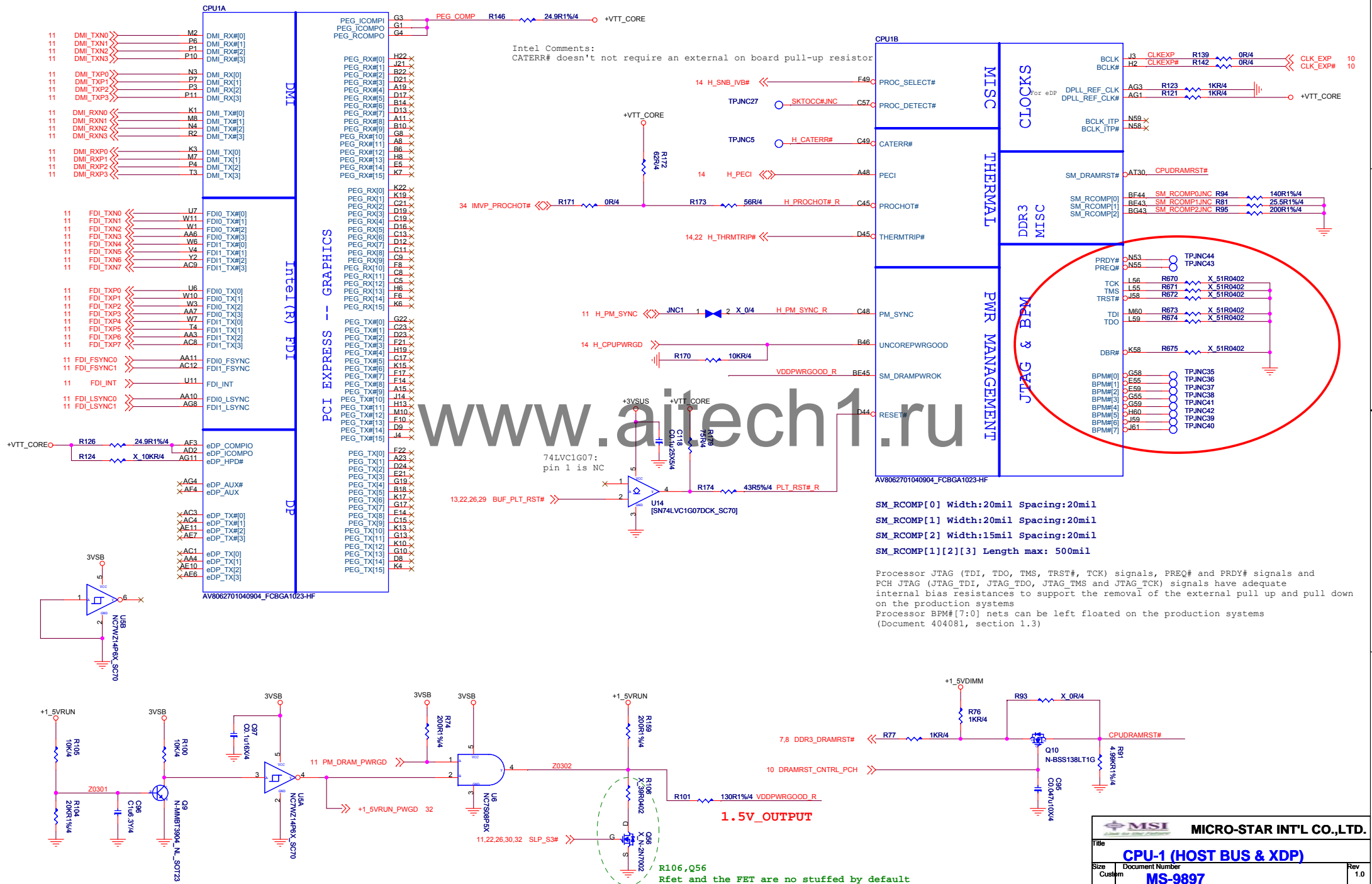
MS-9897 Ver : 1.0

## Huron River Platform

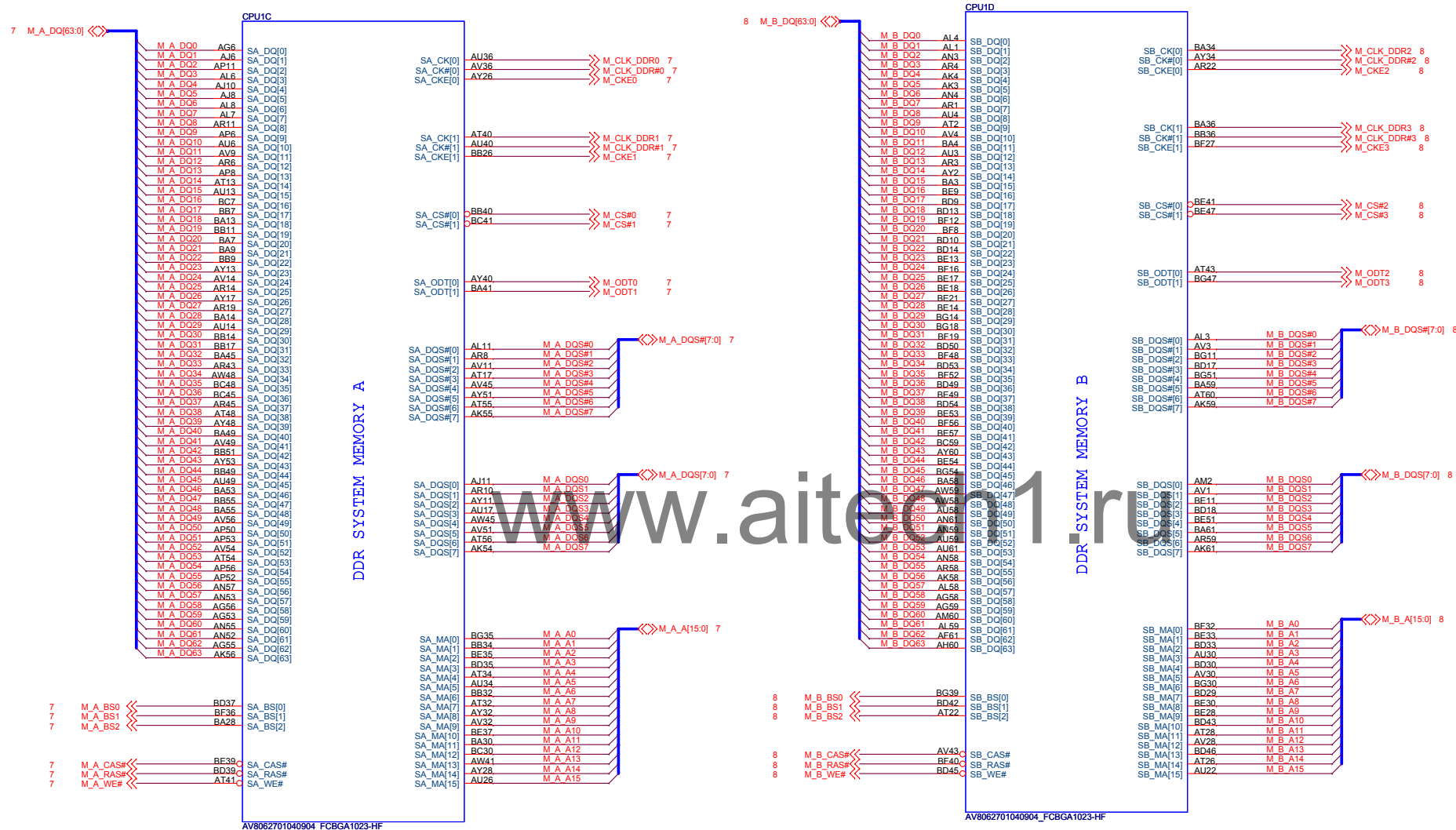
- 01 : BLOCK DIAGRAM
- 02 : CPU-1 (HOST BUS / XDP)
- 03 : CPU-2 (DDR3)
- 04 : CPU-3 (POWER)
- 05 : CPU-4 (GRAPHICS POWER)
- 06 : CPU-5 (GND/RESERVED)
- 07 : DDR3 SODIMM A
- 08 : DDR3 SODIMM B
- 09 : CougarPoint (HDA/JTAG/SATA)
- 10 : CougarPoint (PCI-E/SMBUS/CLK)
- 11 : CougarPoint (DMI/FDI/GPIO)
- 12 : CougarPoint (LVDS/DDI)
- 13 : CougarPoint (PCI/USB/NVRAM)
- 14 : CougarPoint (GPIO/NCTF/RSVD)
- 15 : CougarPoint (POWER)
- 16 : CougarPoint (POWER)
- 17 : CougarPoint (GND)
- 18 : Audio ALC886/887, Amplify APA2051
- 19 : DVI-I
- 20 : HDMI Level shift
- 21 : LVDS
- 22 : SIO-F81866D
- 23 : COM2 -COM6 Connect
- 24 : LAN1 (Intel 82579LM)
- 25 : LAN2 (Intel 82574L)
- 26 : M-SATA/MINI PCI-E SLOT
- 27 : SATA / USB
- 28 : FAN / Front Panel / Buzzer
- 29 : PS2 / Port 80 / TPM1 / DSW / SIM
- 30 : DC IN / 12V Power / Power OK
- 31 : System Power / DC\_IN Detect
- 32 : +1.5VDIMM / VTTDDR\_0.75V
- 33 : +VTT\_CORE / +1\_8VRUN
- 34 : VRM-NCP6131 2 Phase
- 35 : +VCC GFX / +VCC\_CORE
- 36 : +0.85VRUN / +V1.05M\_LAN
- 37 : Power MAP
- 38 : Screw
- 39 : History



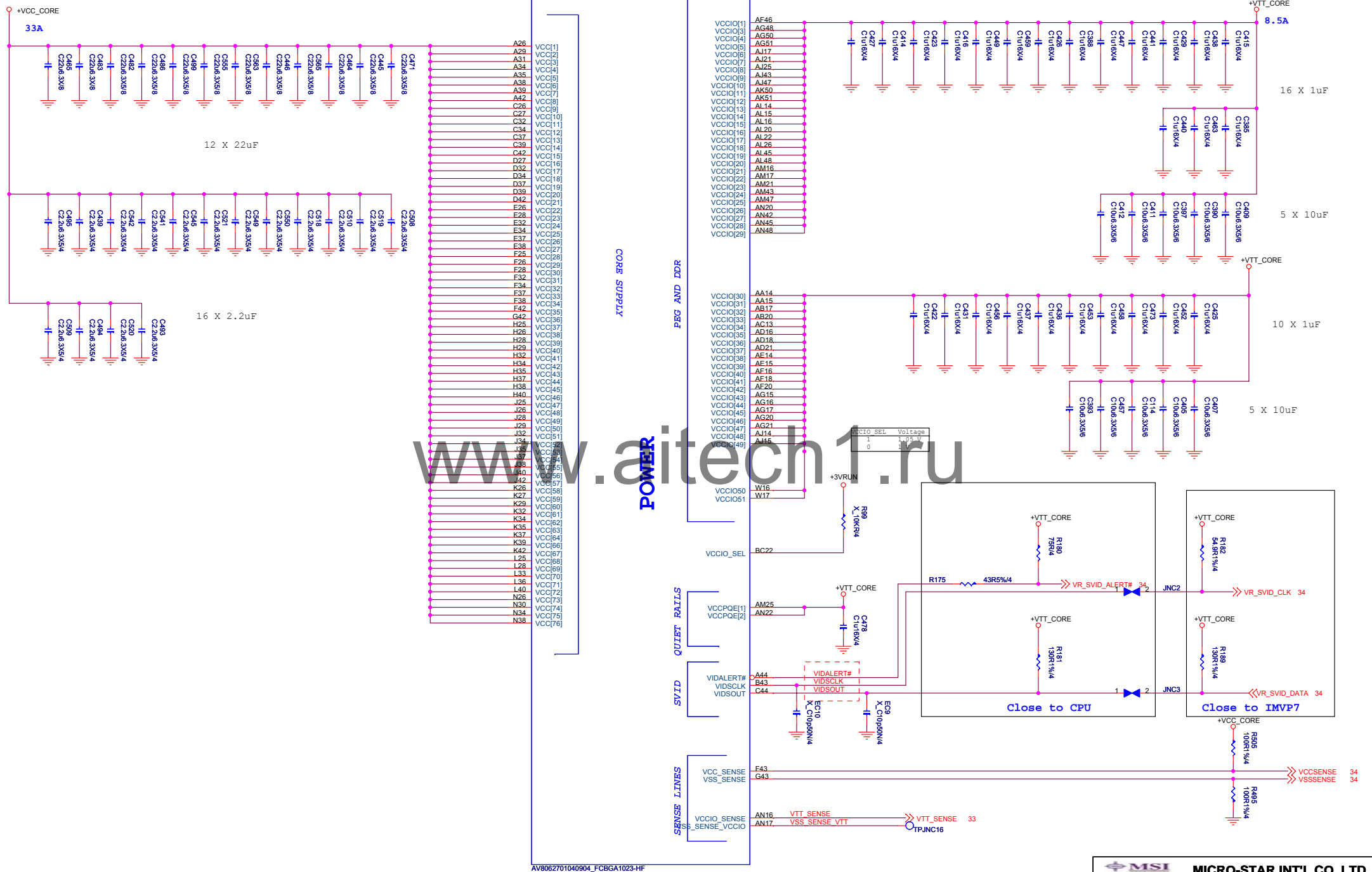
**SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)**



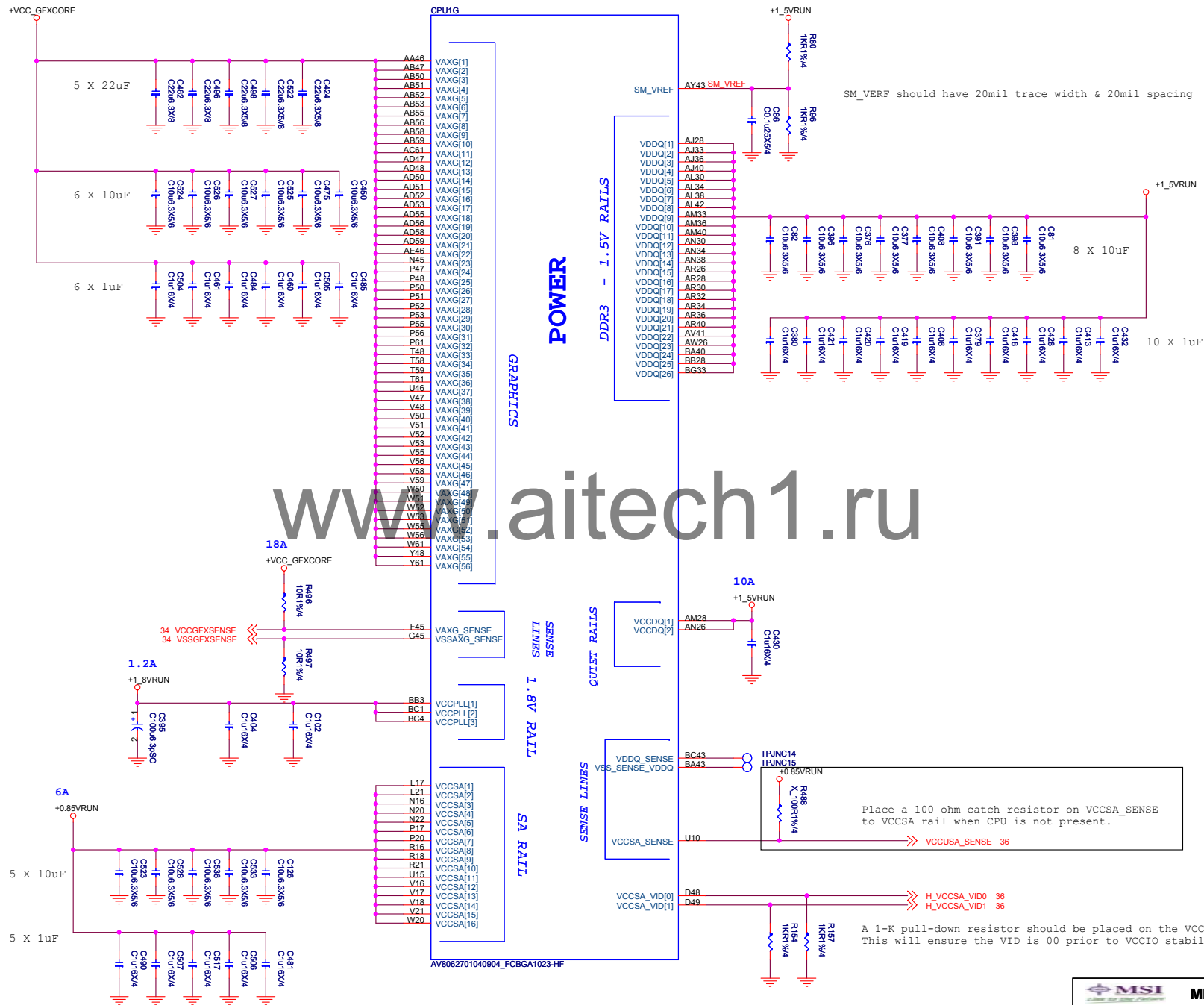
## SANDYBRIDGE PROCESSOR (DDR3)



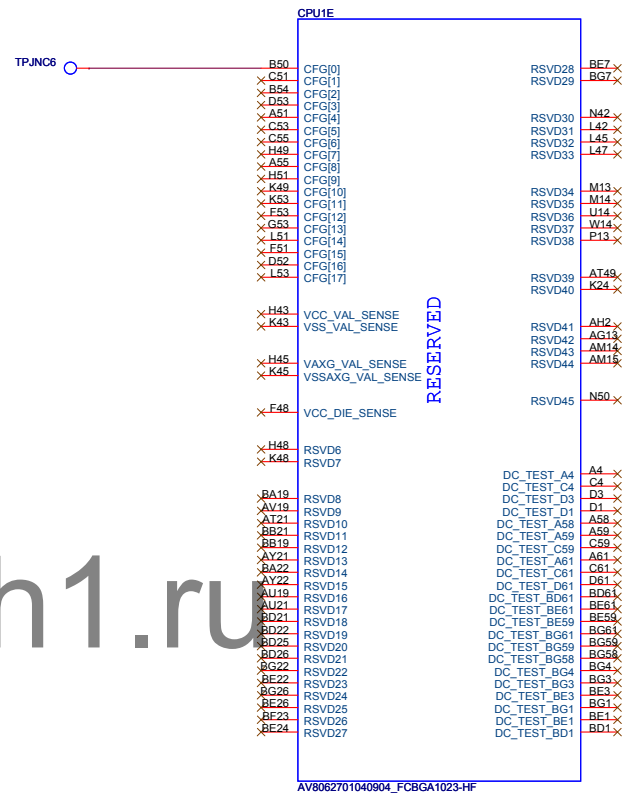
## SANDYBRIDGE PROCESSOR (POWER)



## SANDYBRIDGE PROCESSOR (GRAPHICS POWER)



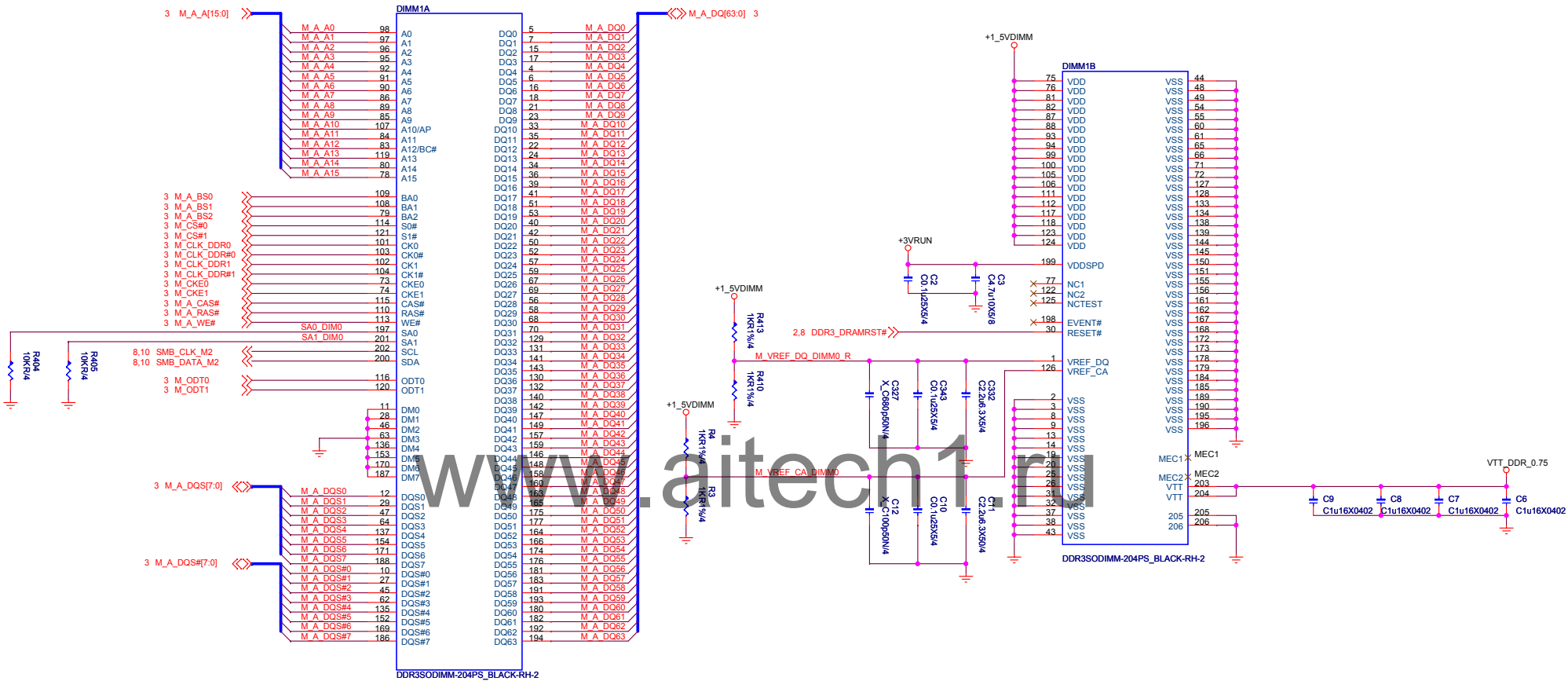
RESERVED



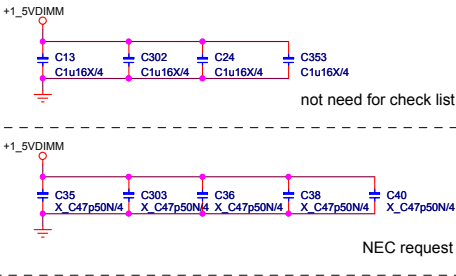
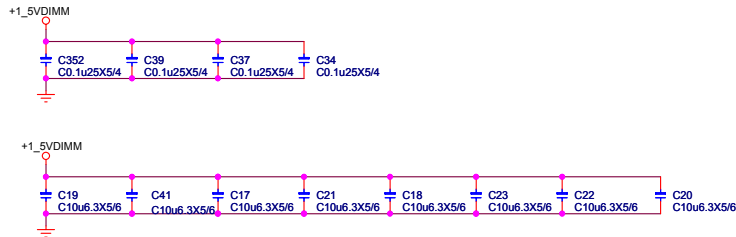
PCI-Express Configuration Select	
CFG[5:6]	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express (Default)



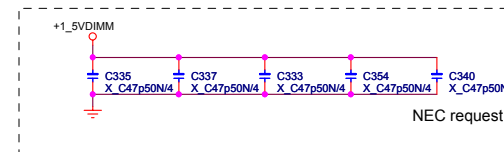
SODIMM#A



close to so-dimm

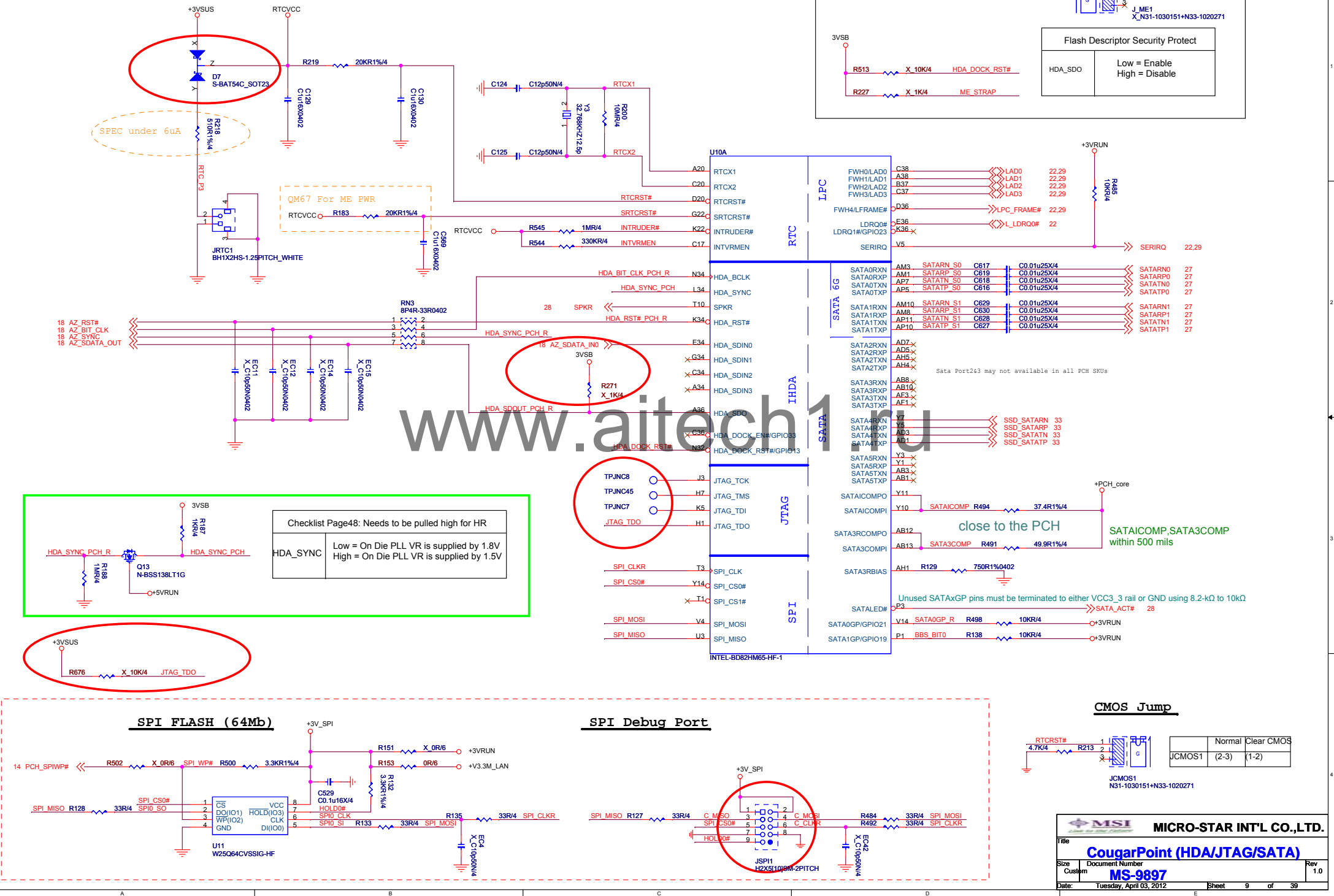


**close to so-dimm**

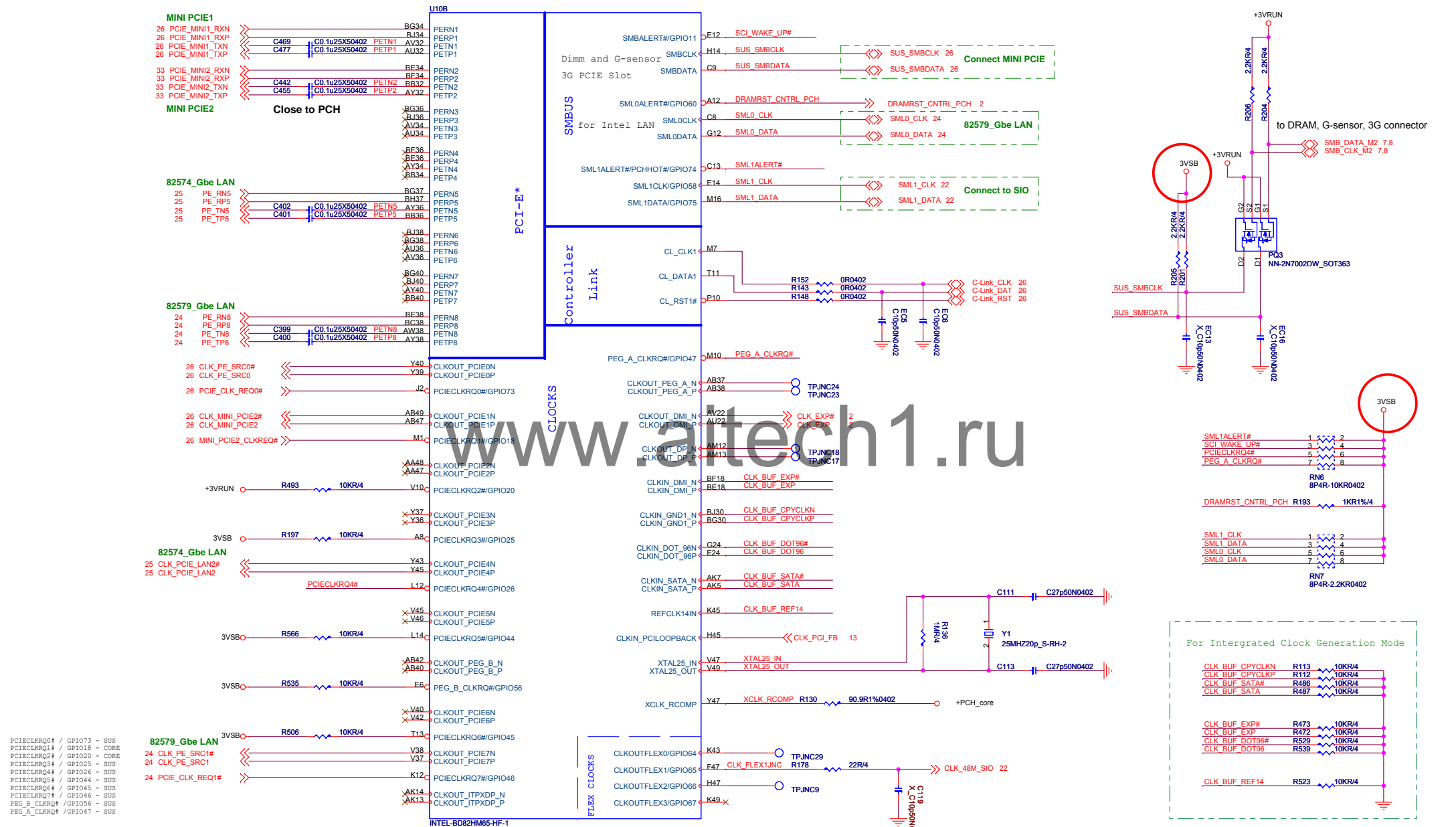




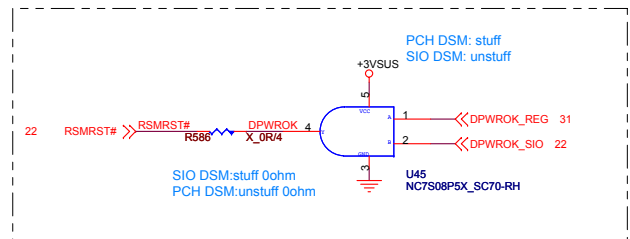
COUGAR POINT (HDA,JTAG,SATA)



# COUGAR POINT (PCI-E, SMBUS, CLK)



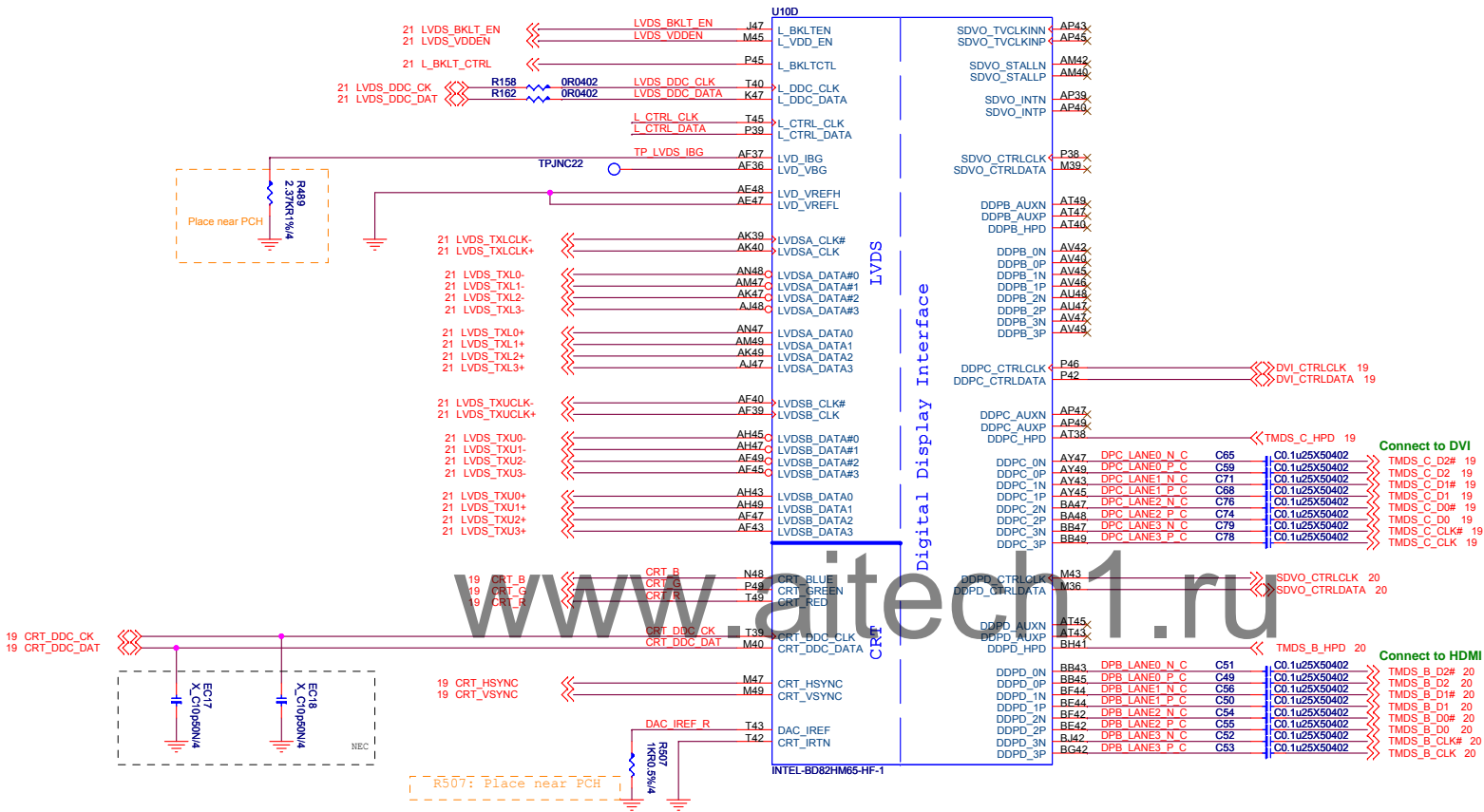
A	B	C	D	E
---	---	---	---	---



```
DPWROK
Without deep s4/s5 support tied together with RSMRST#
EC control
```

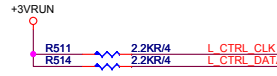
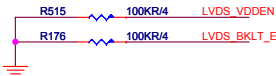
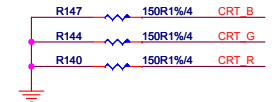


COUGAR POINT (LVDS,DDI)

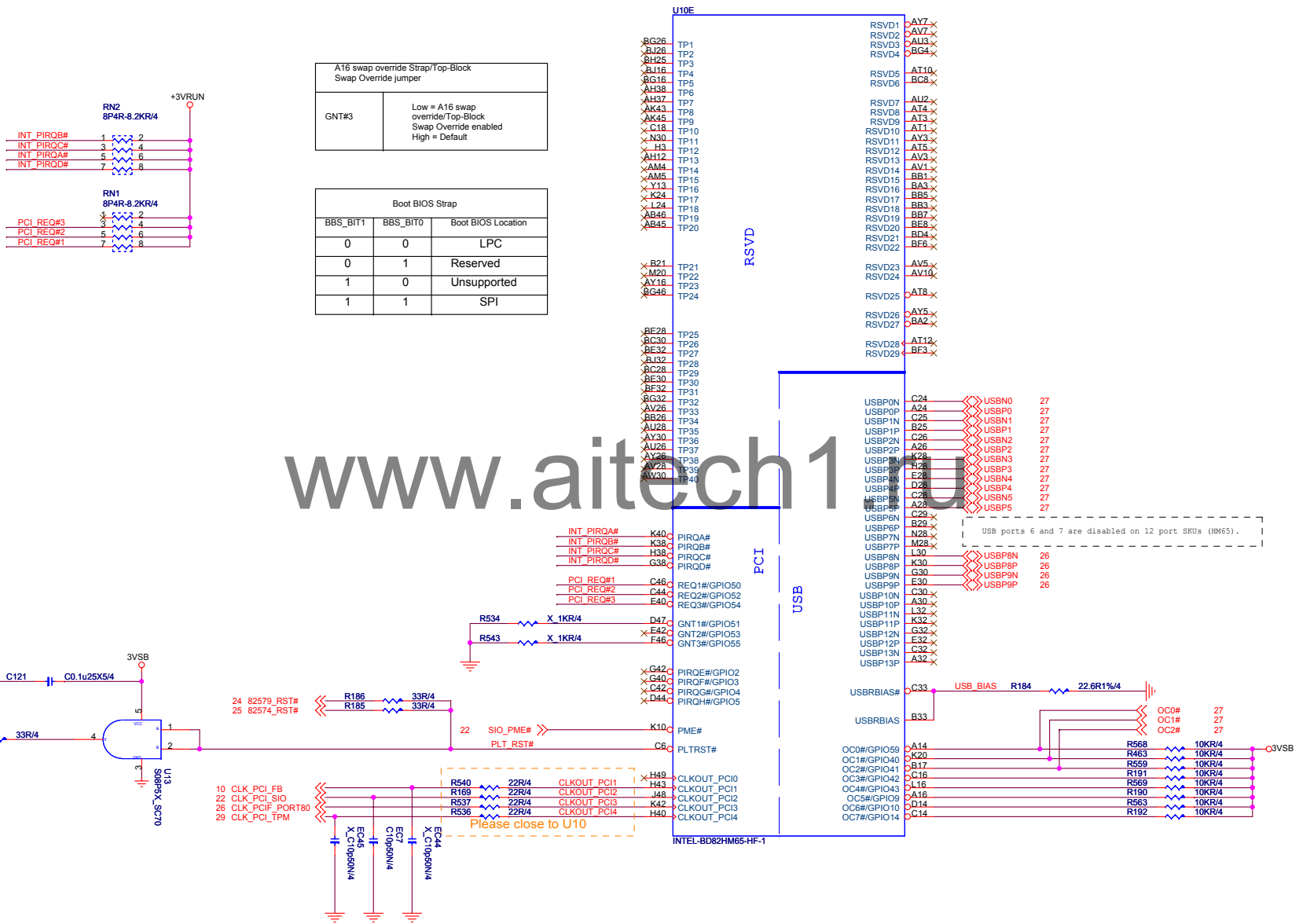


PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-D	DDPD_[0]P	TMDSD_DATA2
	DDPD_[0]N	TMDSD_DATA2#
	DDPD_[1]P	TMDSD_DATA1
	DDPD_[1]N	TMDSD_DATA1#
	DDPD_[2]P	TMDSD_DATA0
	DDPD_[2]N	TMDSD_DATA0#
	DDPD_[3]P	TMDSD_CLK
	DDPD_[3]N	TMDSD_CLK#
	DDPD_AUXP	NA
	DDPD_AUXN	NA
	DDPD_HPDP	HDMID_HPDP
	DDPD_CTRLCLK	HDMID_CTRLCLK
	DDPD_CTRLDATA	HDMID_CTRLDATA

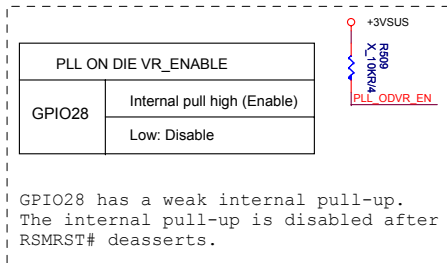
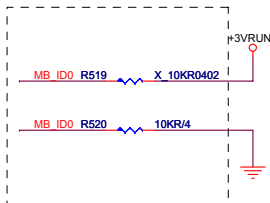
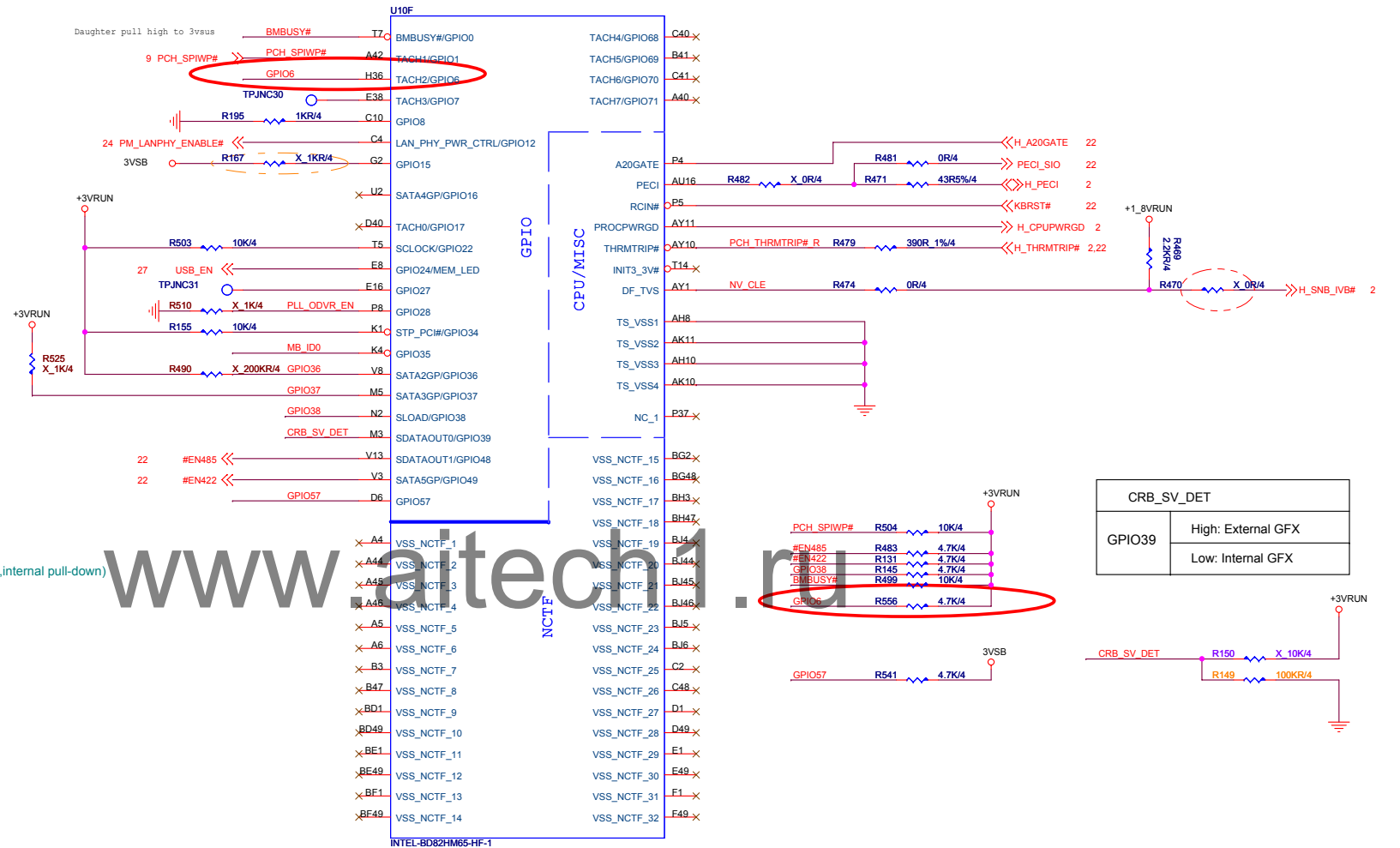
Place the 3 resistors close to PCH



COUGAR POINT (PCI,USB,NVRAM)



# COUGAR POINT (GPIO,NCTF,RSVD)



GPIO36 & GPIO37  
% When Used as SATA2GP/SATA3GP for Mechanical Presence detect -  
Use a weak external pull-up (150K-200K ohms) to Vcc3\_3  
OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

% When Used as GP Input (Pin HW default) -  
Ensure GPI is not driven high during strap sampling window

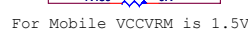
%When Unused as GPIO or SATA\*GP -  
Use 8.2K-10K pull-down to ground.

Check list 1.5  
Reserved.  
This signal has a weak internal pull-down.  
NOTE: The internal pull-down is disabled after PLTRST# deasserts.  
NOTE: This signal should not be pulled high when strap is sampled.

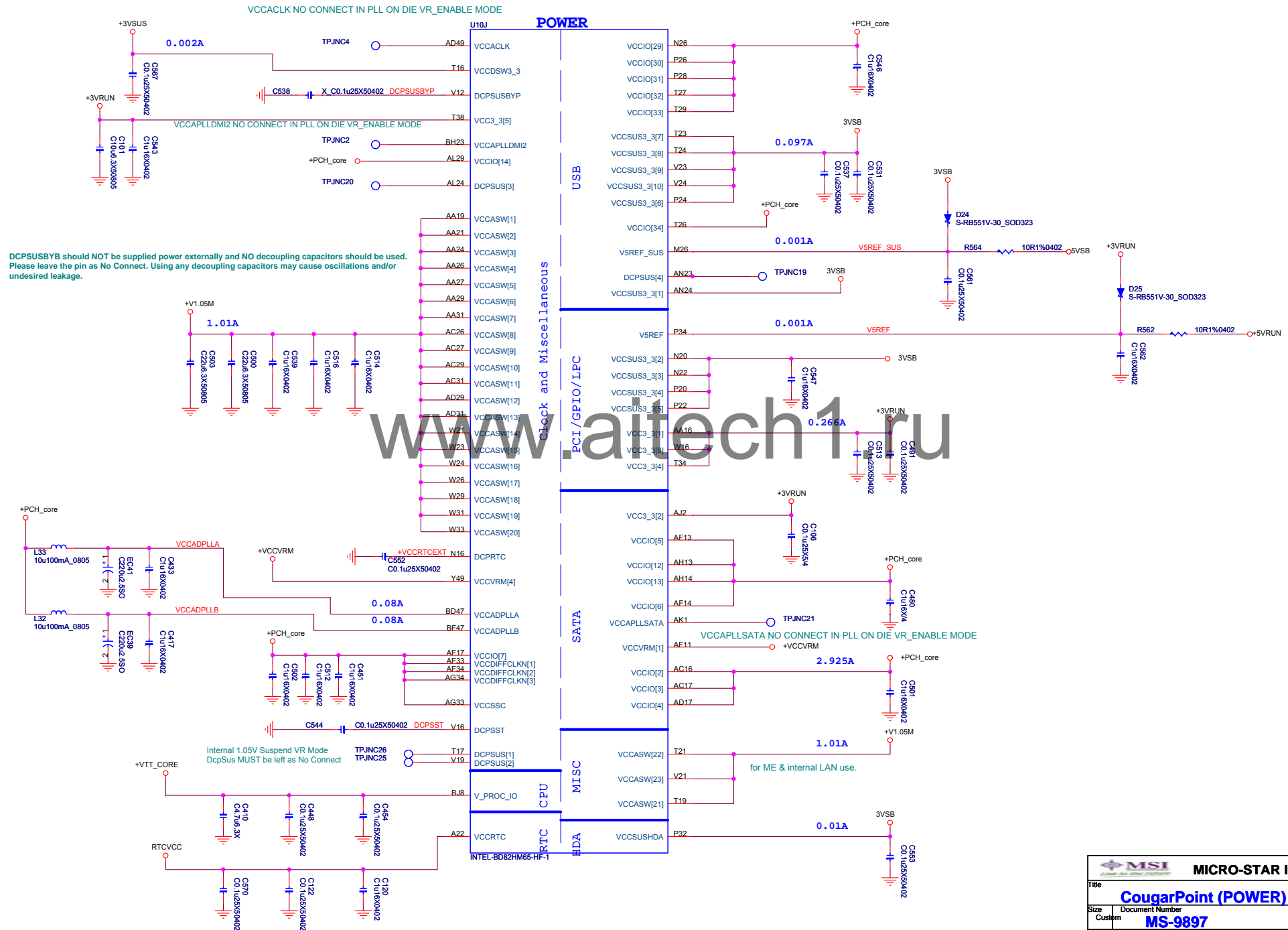


The screenshot shows a portion of a PCB layout with a power plane. Various voltage levels and current densities are indicated:

- VCCIO[22]**: 0.02A
- VCCIO[23]**: 0.02A
- VCCIO[24]**: 0.02A
- VCCIO[25]**: 0.19A
- VCCIO[26]**: 0.02A
- VCCIO[27]**: 0.02A
- VCCIO[28]**: 0.02A
- VCCIO[29]**: 0.02A
- VCCIO[30]**: 0.02A
- VCCIO[31]**: 0.02A
- VCCIO[32]**: 0.02A
- VCCIO[33]**: 0.02A
- VCCIO[34]**: 0.02A
- VCCIO[35]**: 0.02A
- VCCIO[36]**: 0.02A
- VCCIO[37]**: 0.02A
- VCCIO[38]**: 0.02A
- VCCIO[39]**: 0.02A
- VCCIO[40]**: 0.02A
- VCCIO[41]**: 0.02A
- VCCIO[42]**: 0.02A
- VCCIO[43]**: 0.02A
- VCCIO[44]**: 0.02A
- VCCIO[45]**: 0.02A
- VCCIO[46]**: 0.02A
- VCCIO[47]**: 0.02A
- VCCIO[48]**: 0.02A
- VCCIO[49]**: 0.02A
- VCCIO[50]**: 0.02A
- VCCIO[51]**: 0.02A
- VCCIO[52]**: 0.02A
- VCCIO[53]**: 0.02A
- VCCIO[54]**: 0.02A
- VCCIO[55]**: 0.02A
- VCCIO[56]**: 0.02A
- VCCIO[57]**: 0.02A
- VCCIO[58]**: 0.02A
- VCCIO[59]**: 0.02A
- VCCIO[60]**: 0.02A
- VCCIO[61]**: 0.02A
- VCCIO[62]**: 0.02A
- VCCIO[63]**: 0.02A
- VCCIO[64]**: 0.02A
- VCCIO[65]**: 0.02A
- VCCIO[66]**: 0.02A
- VCCIO[67]**: 0.02A
- VCCIO[68]**: 0.02A
- VCCIO[69]**: 0.02A
- VCCIO[70]**: 0.02A
- VCCIO[71]**: 0.02A
- VCCIO[72]**: 0.02A
- VCCIO[73]**: 0.02A
- VCCIO[74]**: 0.02A
- VCCIO[75]**: 0.02A
- VCCIO[76]**: 0.02A
- VCCIO[77]**: 0.02A
- VCCIO[78]**: 0.02A
- VCCIO[79]**: 0.02A
- VCCIO[80]**: 0.02A
- VCCIO[81]**: 0.02A
- VCCIO[82]**: 0.02A
- VCCIO[83]**: 0.02A
- VCCIO[84]**: 0.02A
- VCCIO[85]**: 0.02A
- VCCIO[86]**: 0.02A
- VCCIO[87]**: 0.02A
- VCCIO[88]**: 0.02A
- VCCIO[89]**: 0.02A
- VCCIO[90]**: 0.02A
- VCCIO[91]**: 0.02A
- VCCIO[92]**: 0.02A
- VCCIO[93]**: 0.02A
- VCCIO[94]**: 0.02A
- VCCIO[95]**: 0.02A
- VCCIO[96]**: 0.02A
- VCCIO[97]**: 0.02A
- VCCIO[98]**: 0.02A
- VCCIO[99]**: 0.02A



COUGAR POINT (POWER)

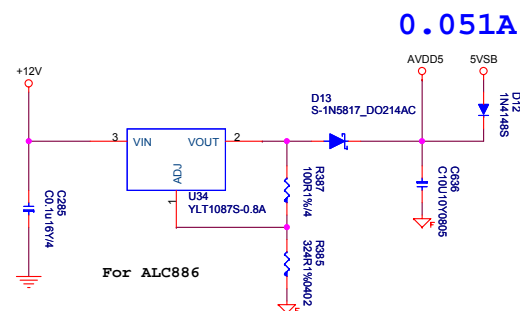


# Cougar Point (GND)

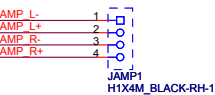
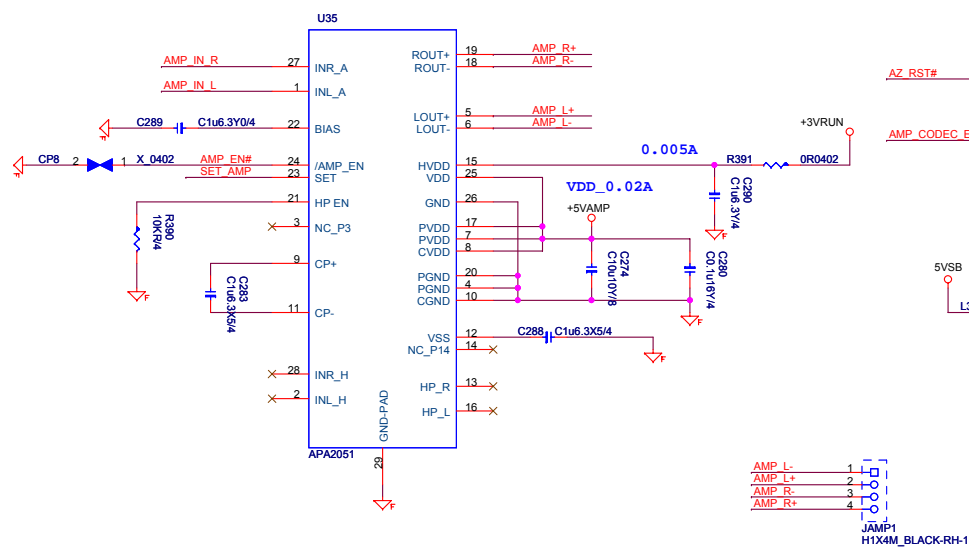


www.aitech1.ru

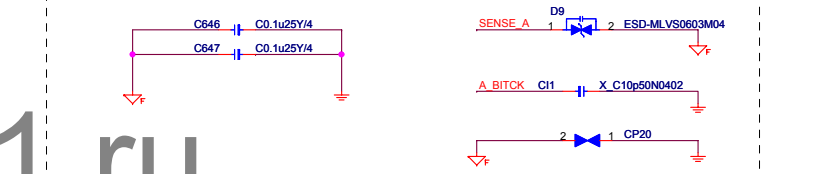
## AUDIO CODE REGULATORS

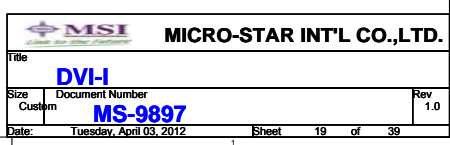


## Amplify

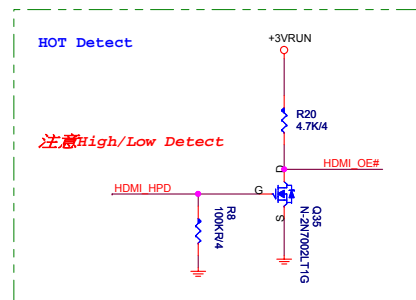
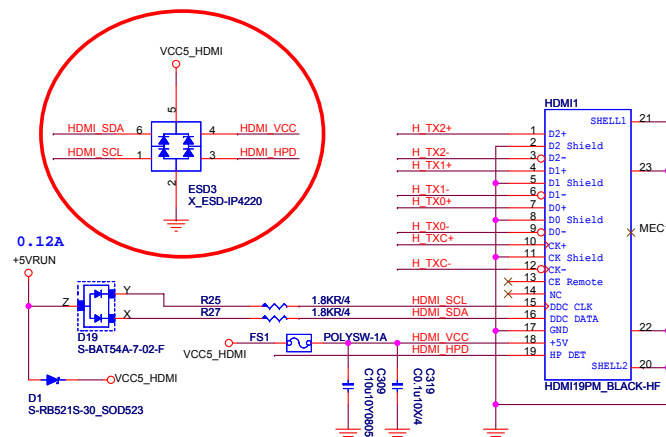
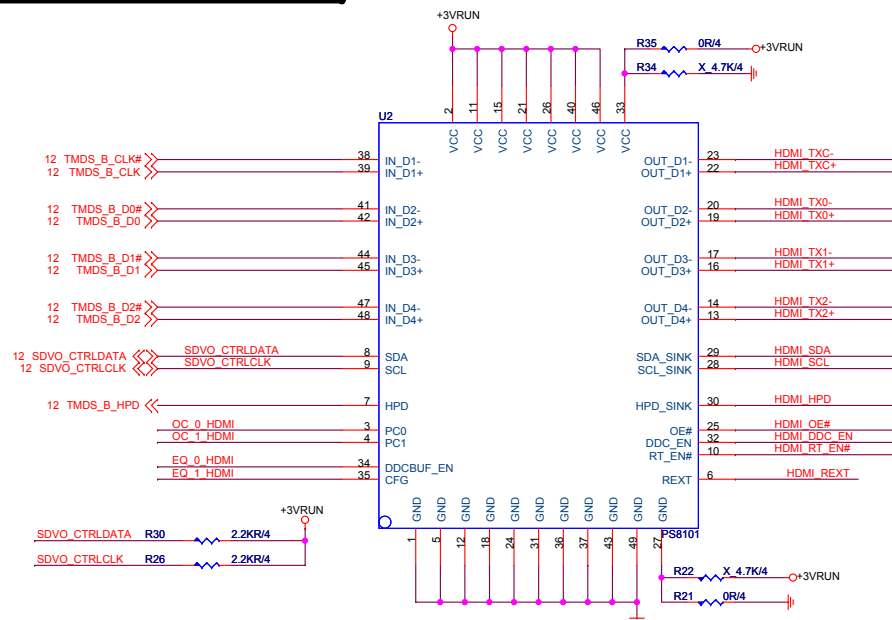


## For EMI

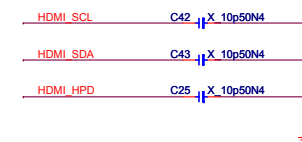
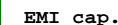
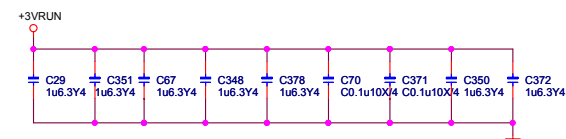
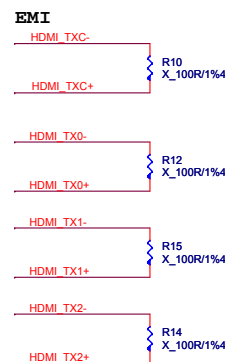
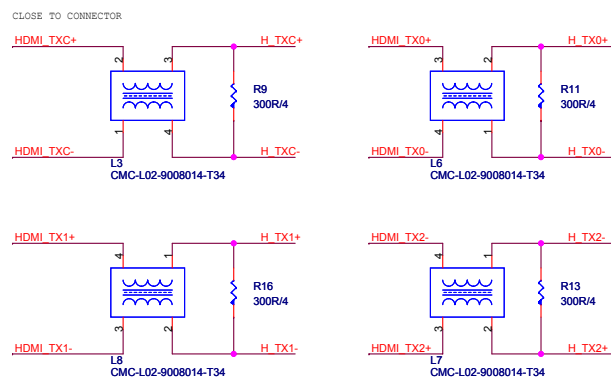
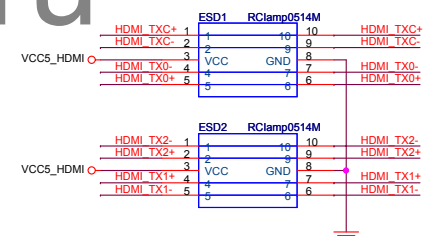
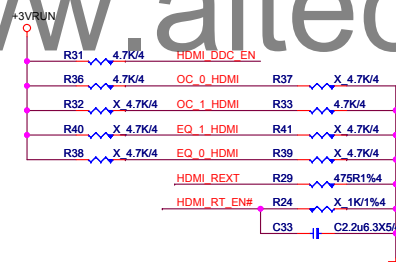




## HDMI level shifter

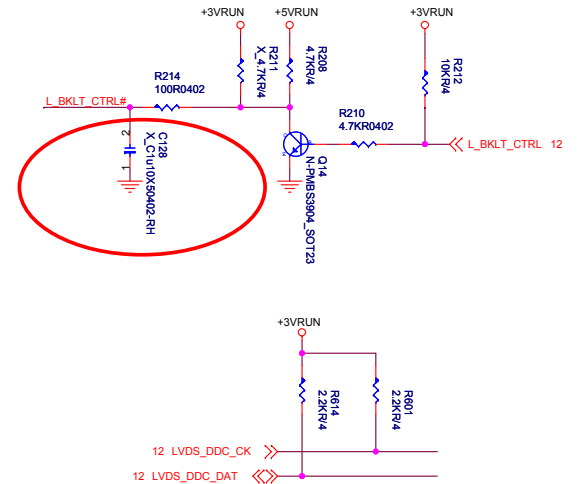
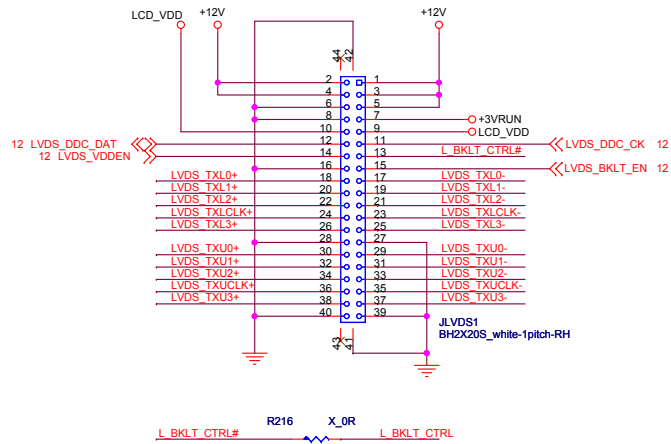
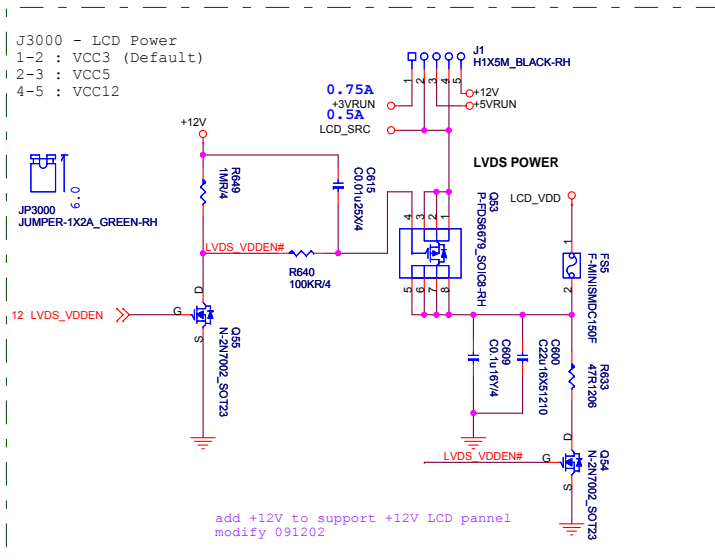


www.aitech1.ru



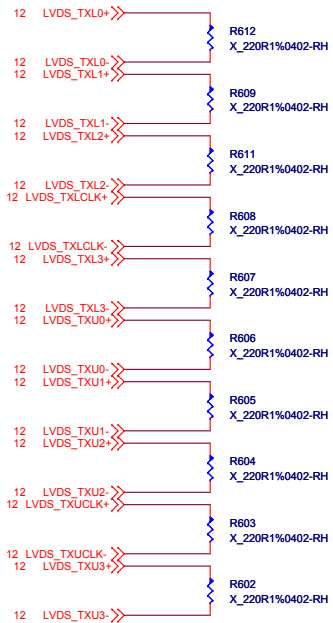


## LVDS PIN HEADER



[www.aitech1.ru](http://www.aitech1.ru)

Close to JLVDS3000

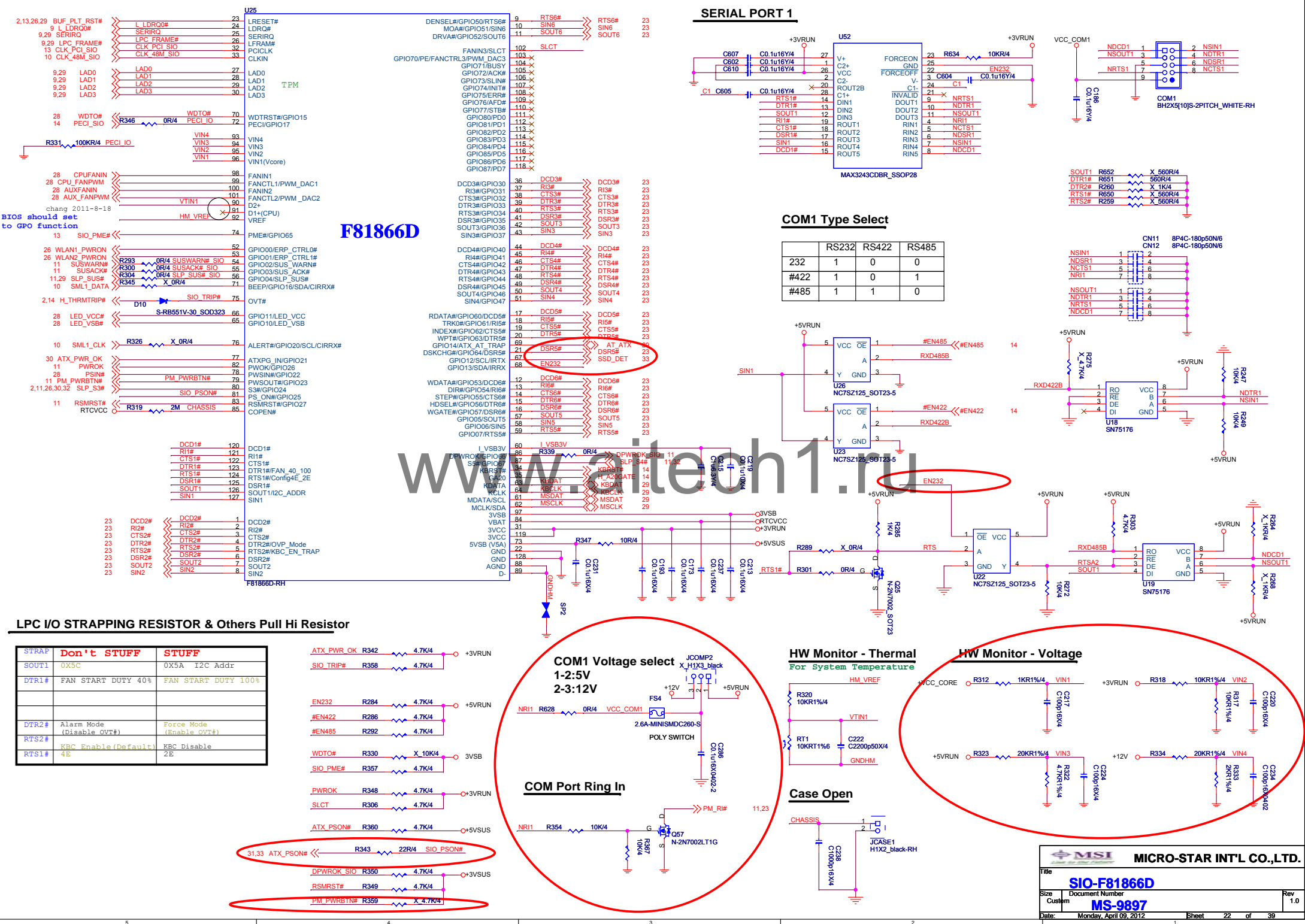


## LEVEL SHIFT

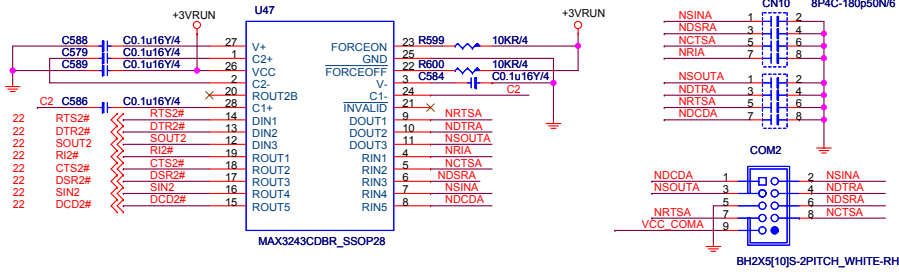
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUP_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

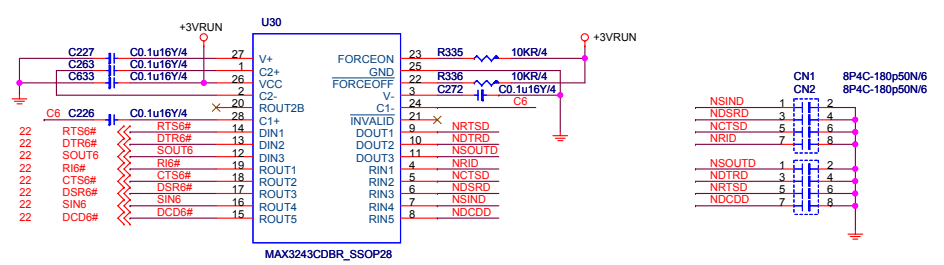
PC1, PC0		note
00	8 dB	internal pull-down at ~ 500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	



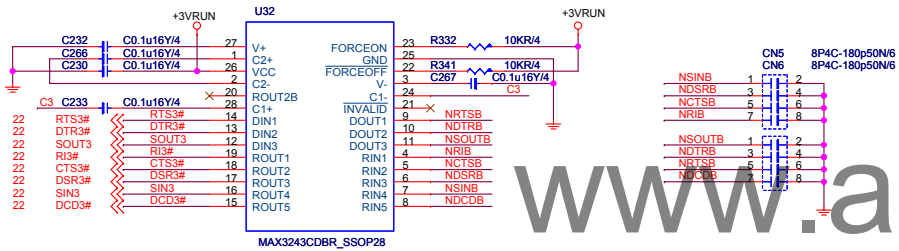
## COM PORT 2



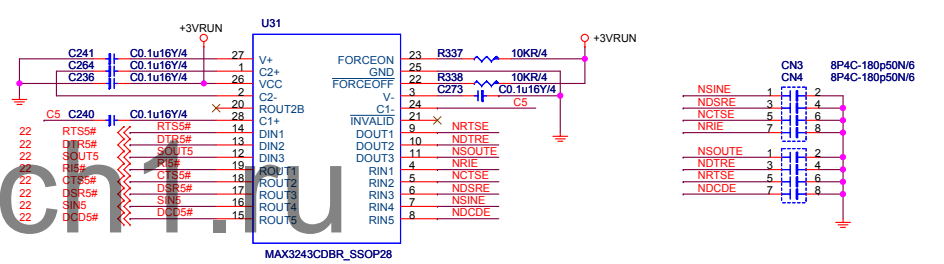
## COM PORT 6



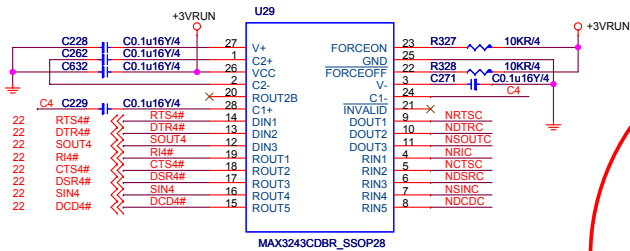
## COM PORT 3



## COM PORT 5

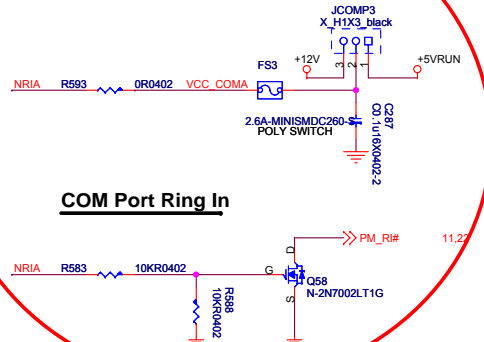


## COM PORT 4

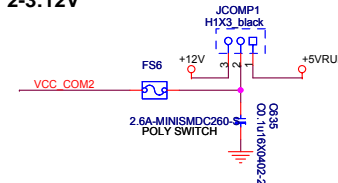


COM2 Voltage select  
1-2:5V  
2-3:12V

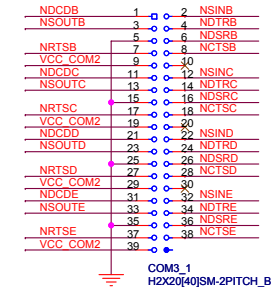
COM Port Ring In

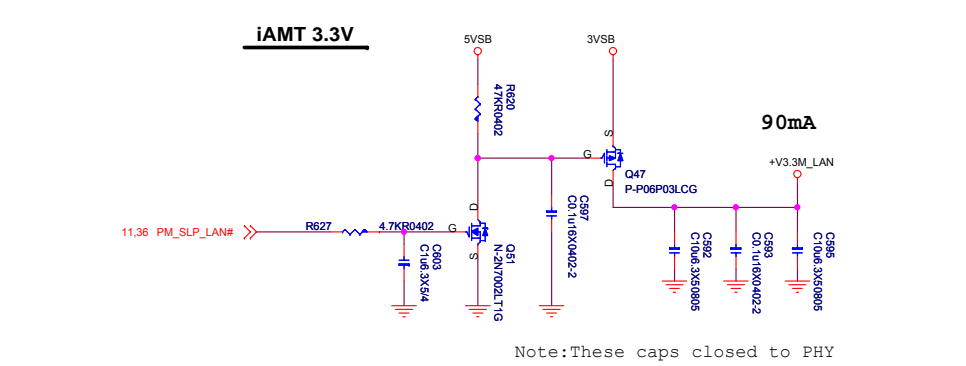
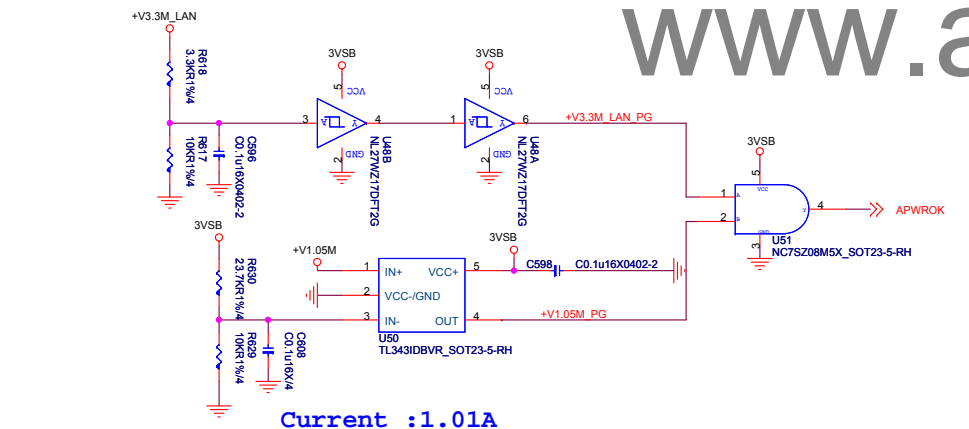
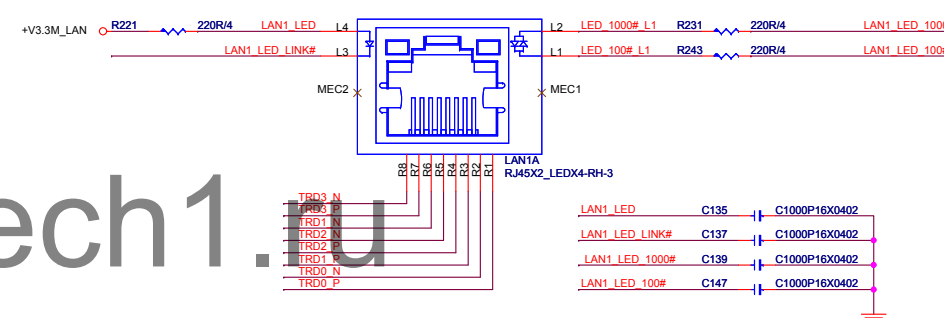
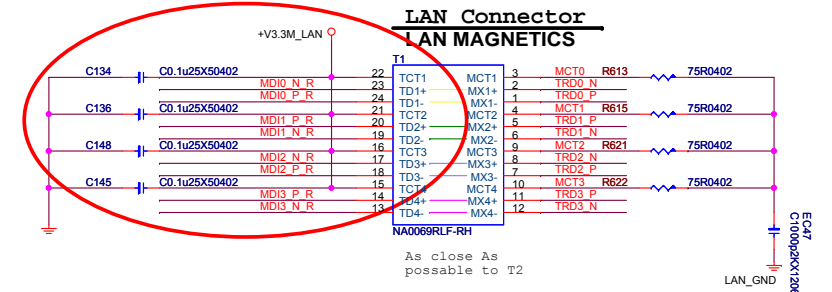
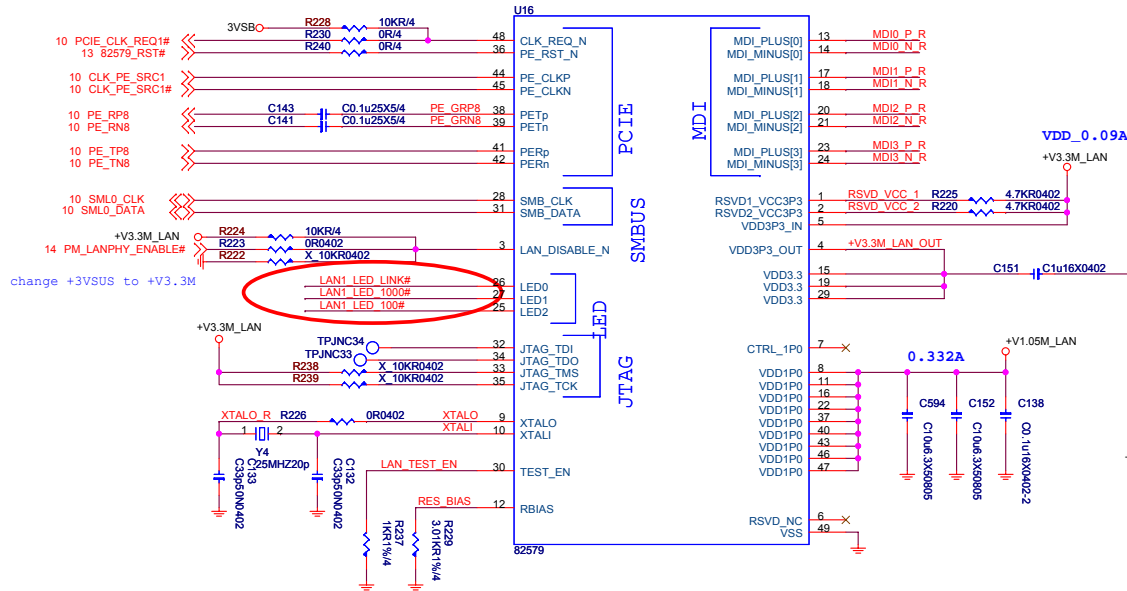


COM3-6 Voltage select  
1-2:5V  
2-3:12V

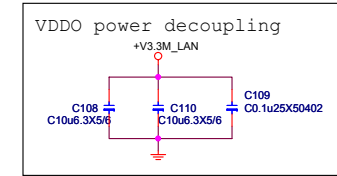


COMB-E Connect





Giga-Lan	
N58-22P0221-842	
Link	Yellow
Active	Blinking
1000	Orange
100	Green
10	None
L4	
L3	Yellow
L2	Orange
L1	Green

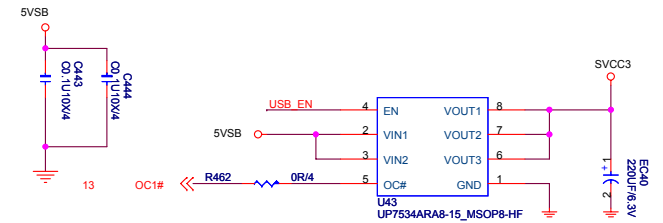
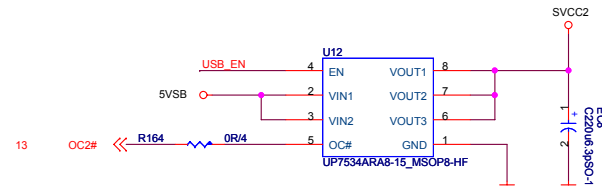
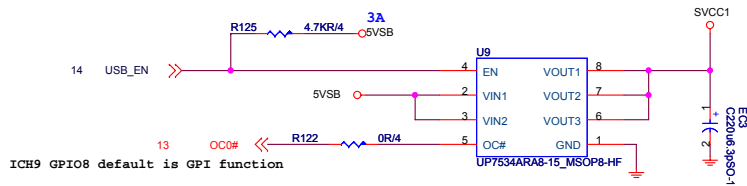




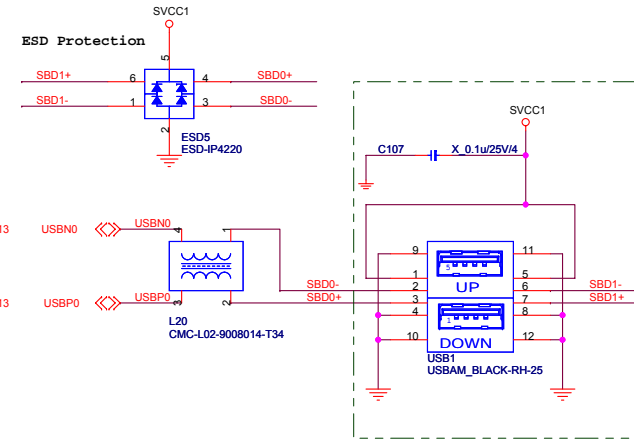




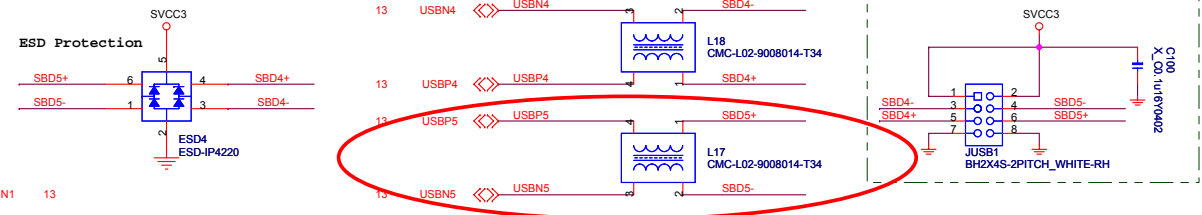
EMI suggest use uP7534ARA8-15



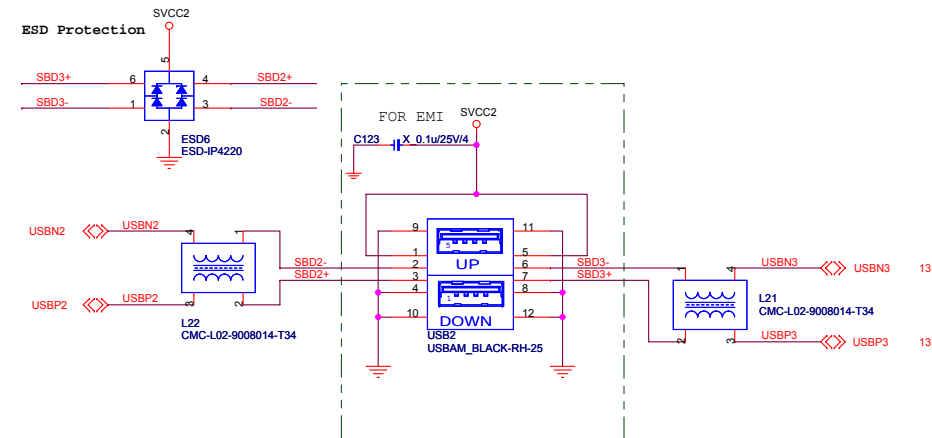
## REAR PANEL USB CONNECTOR FOR USB PORT 0,1



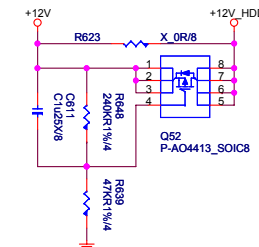
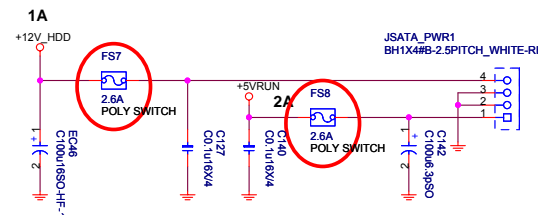
## FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



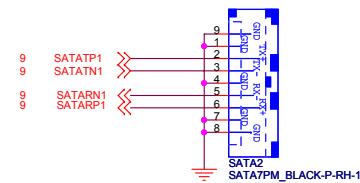
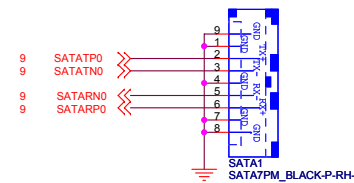
## REAR PANEL USB CONNECTOR FOR USB PORT 2,3



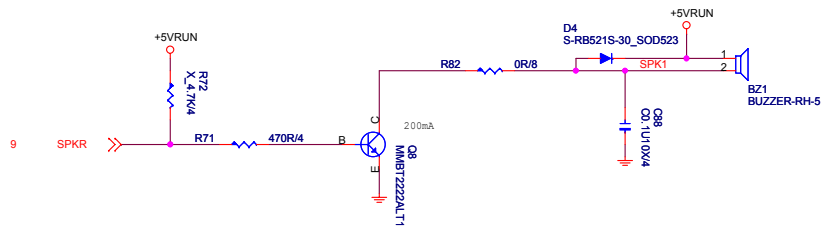
## SATA Power



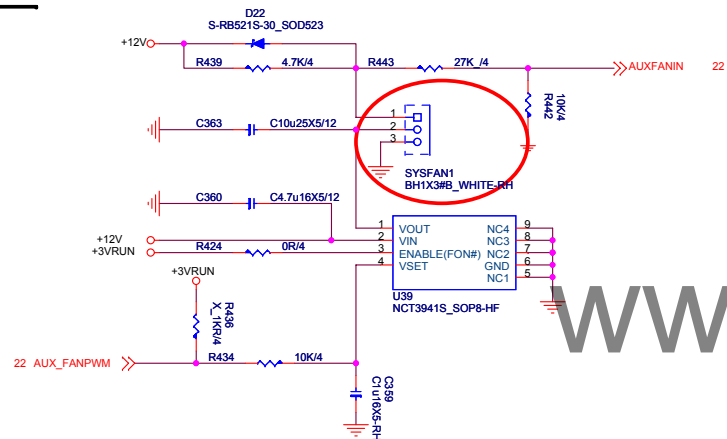
## SATA Conn



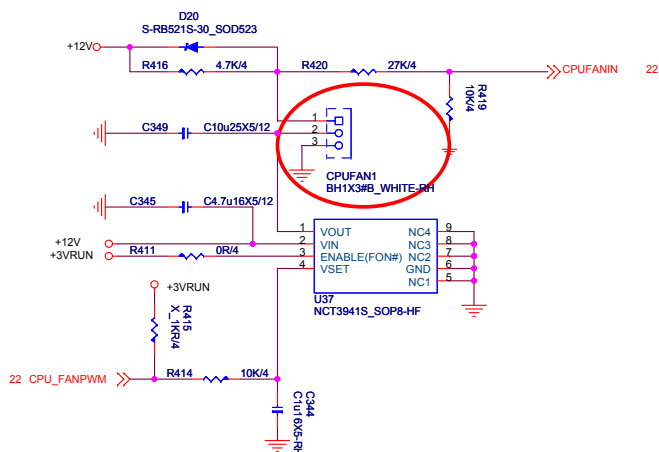
## Buzzer



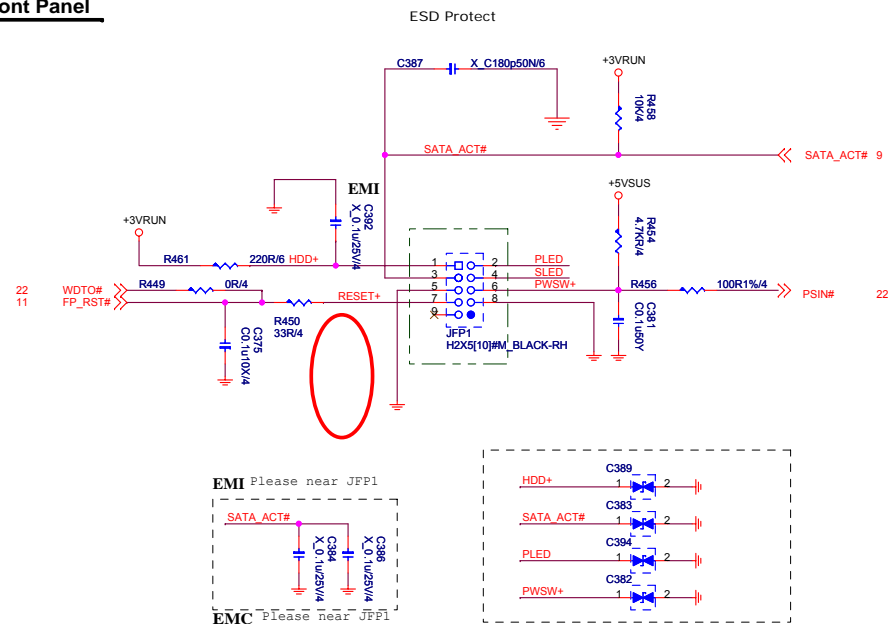
## SYS FAN



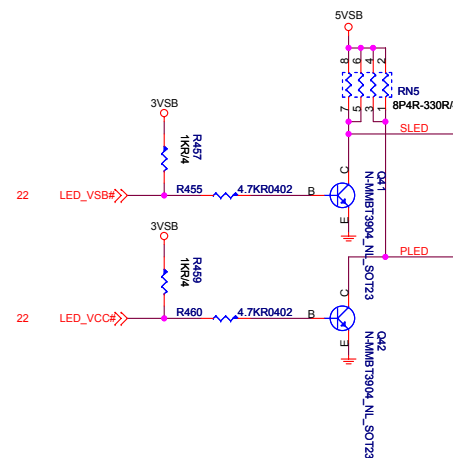
## CPU FAN



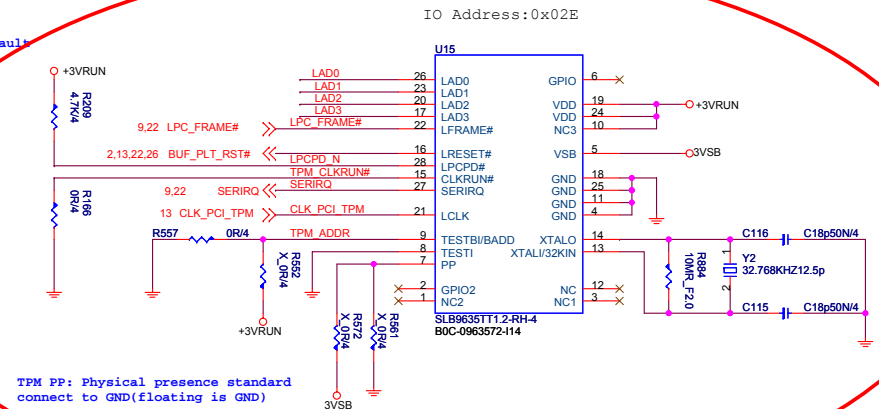
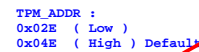
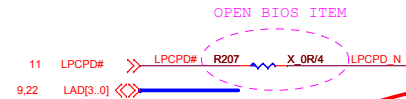
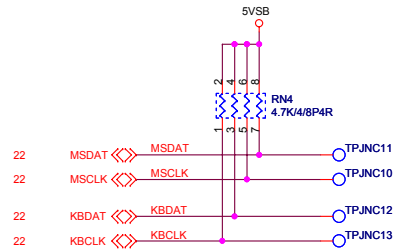
## Intel Front Panel



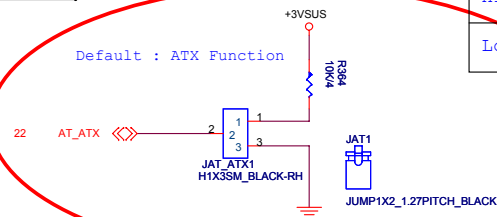
## LED (for Fintek 81866D)



AT\_ATX



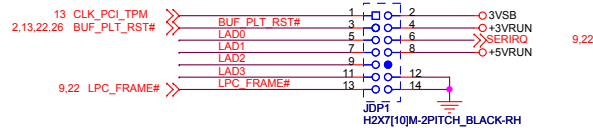
TPM PP: Physical presence standard  
connect to GND(floating is GND)



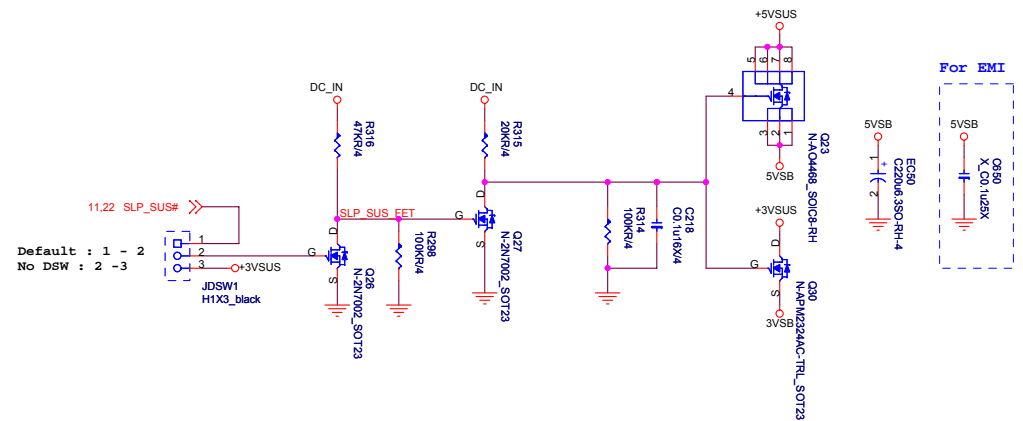
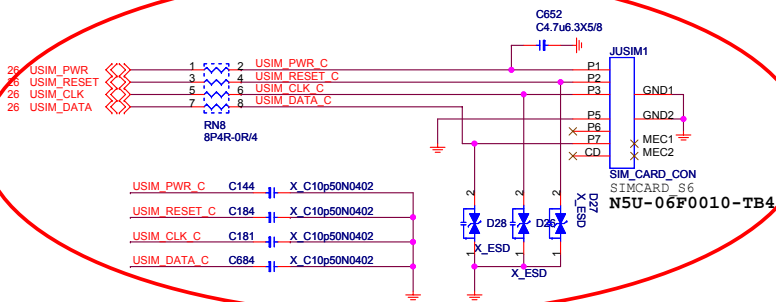
High	ATX-Function Pin-1,2
Low	AT-Function Pin-2,3

www.aitech1.ru

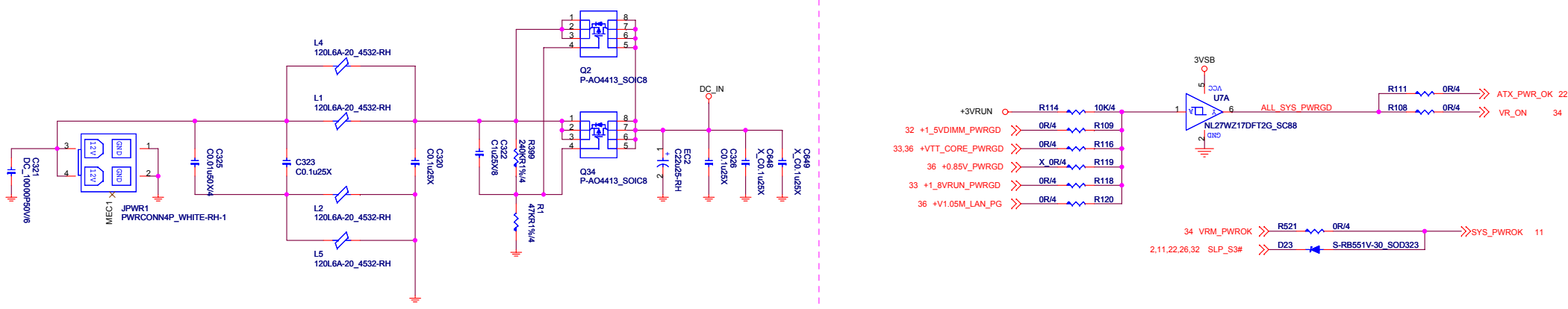
9,22 LAD[3..0] <<>



Default : 1 - 2  
No DSW : 2 -3

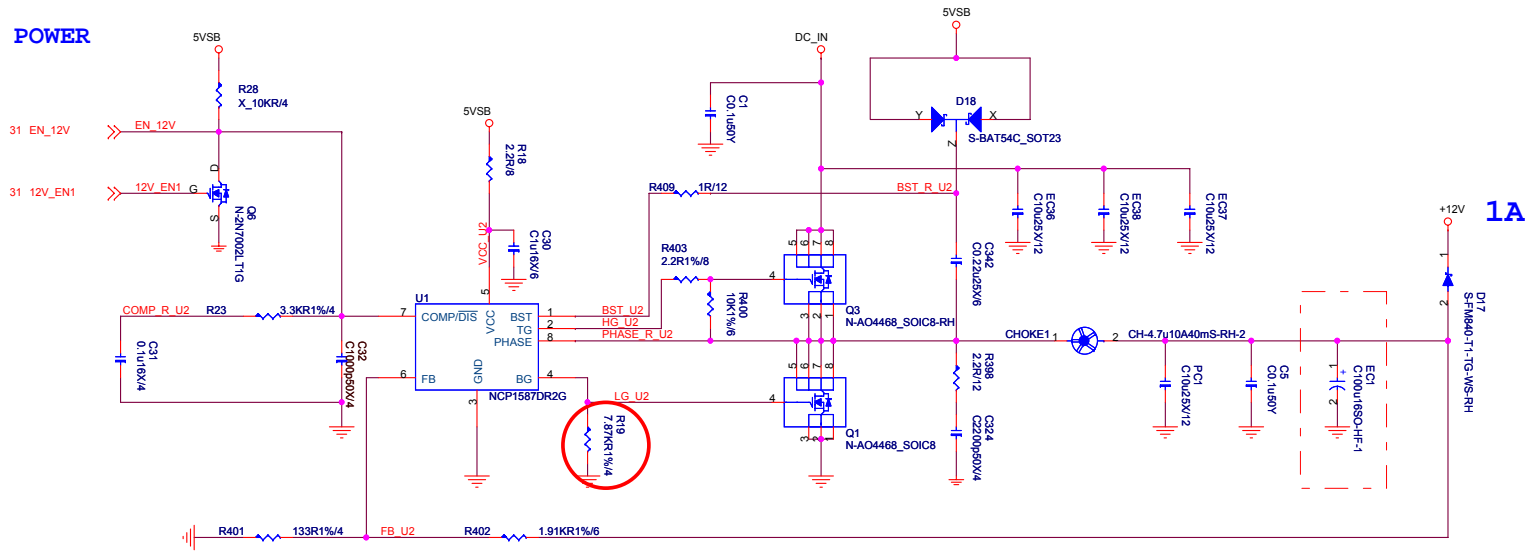


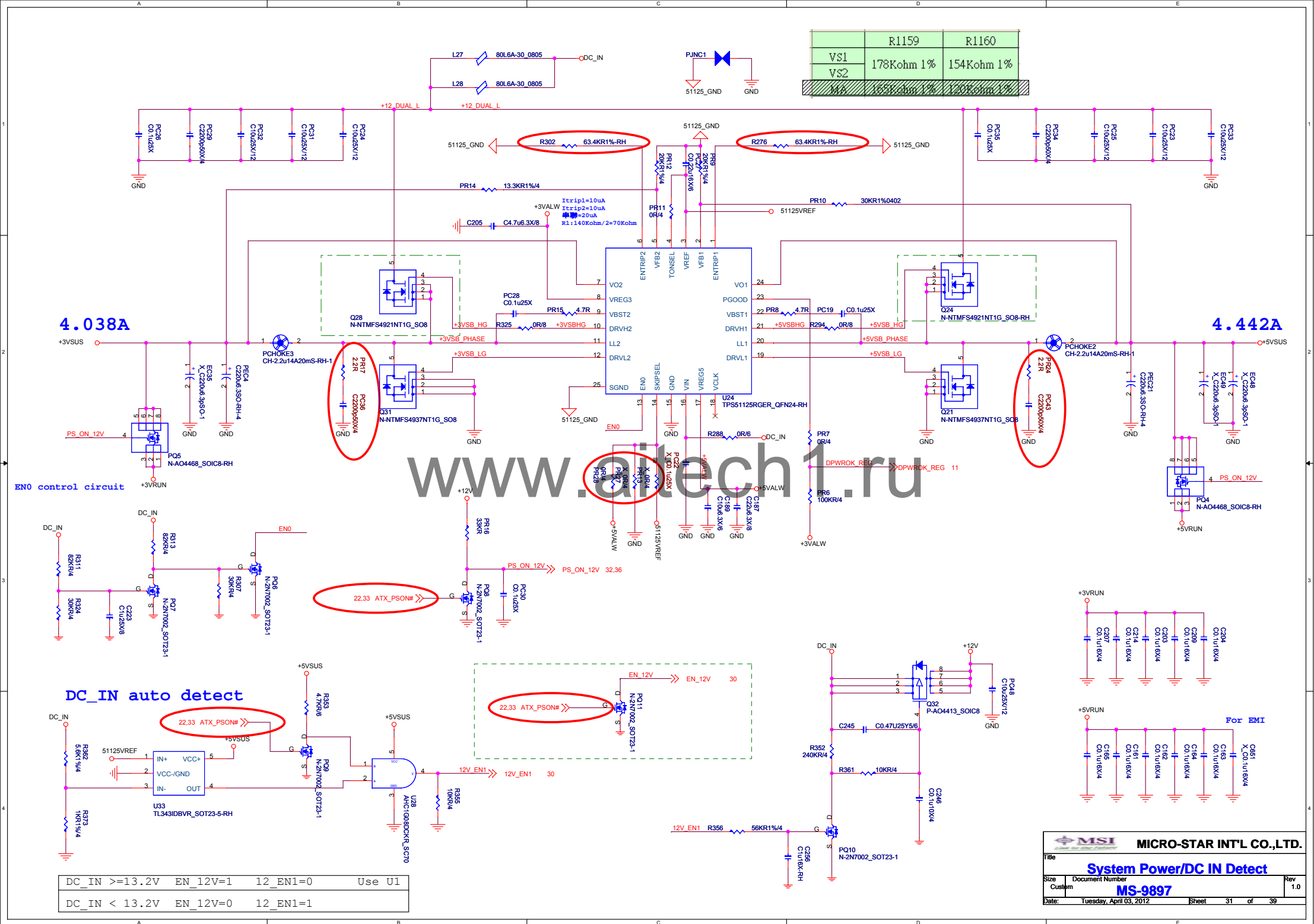
For EMI



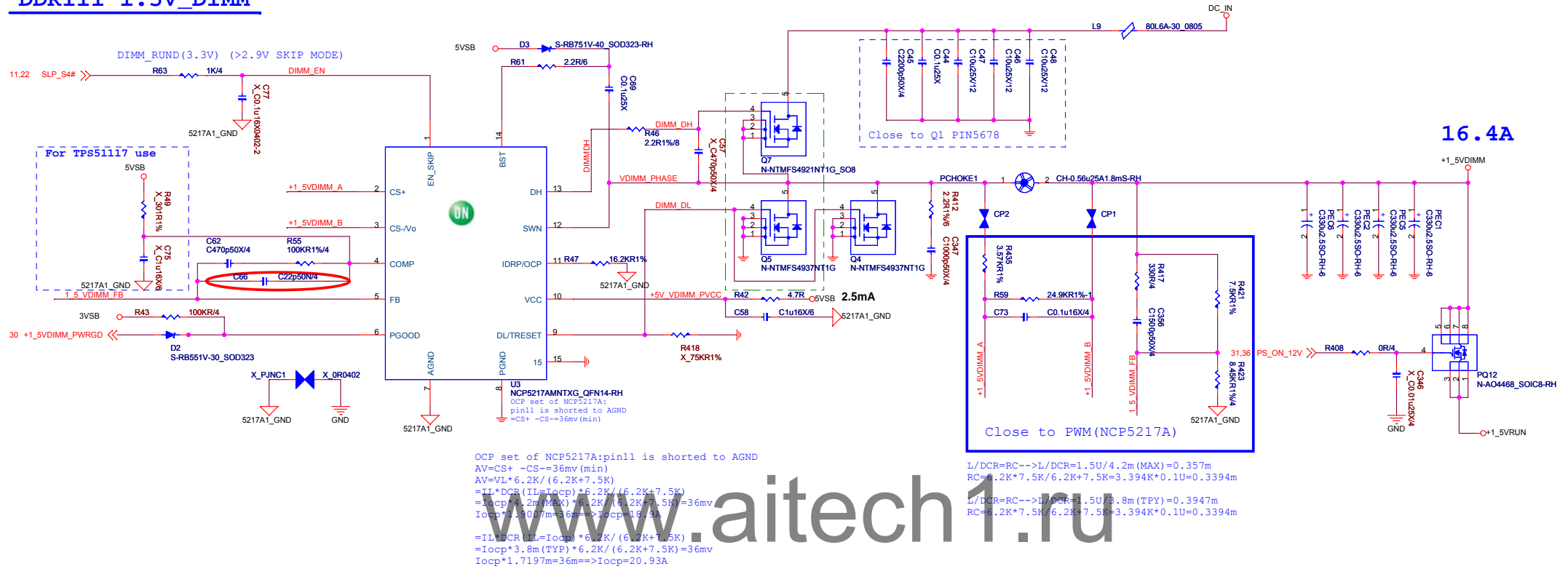
www.aitech1.ru

+12V POWER

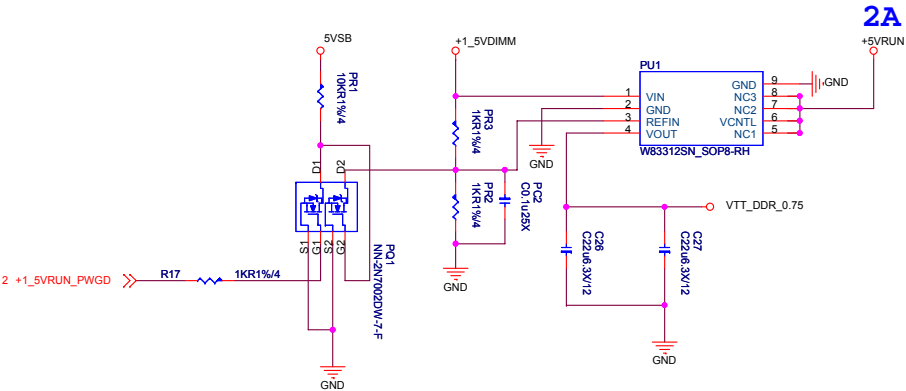




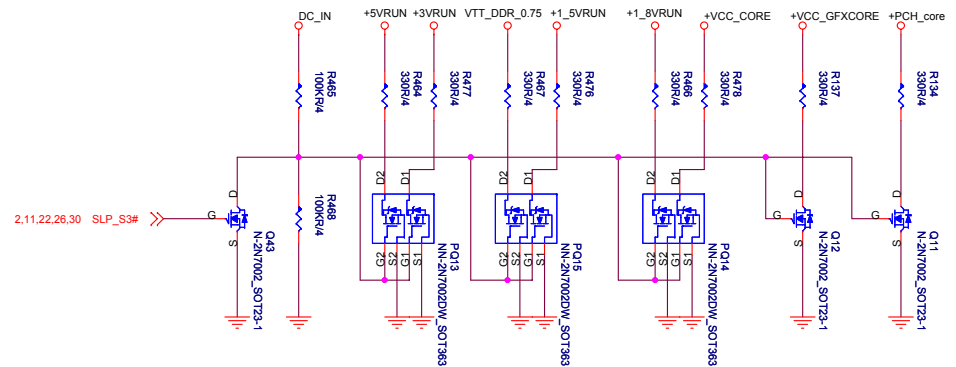
DDRIII 1.5V\_DIMM



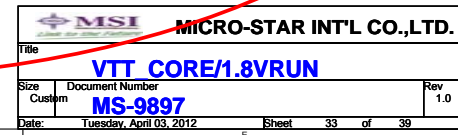
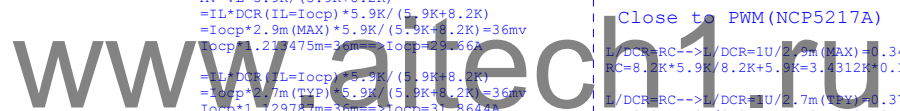
## VTT\_DDR\_0.75

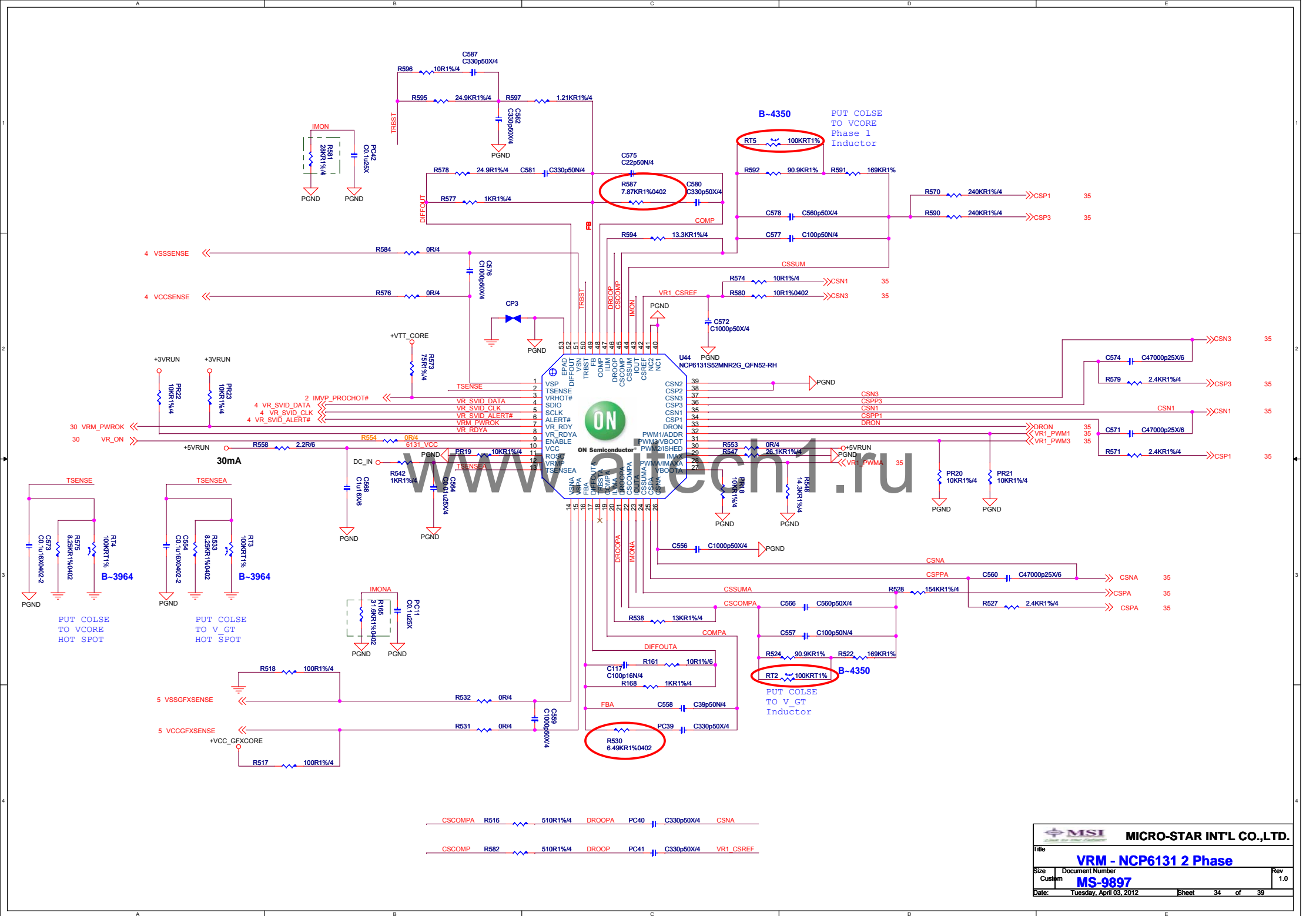


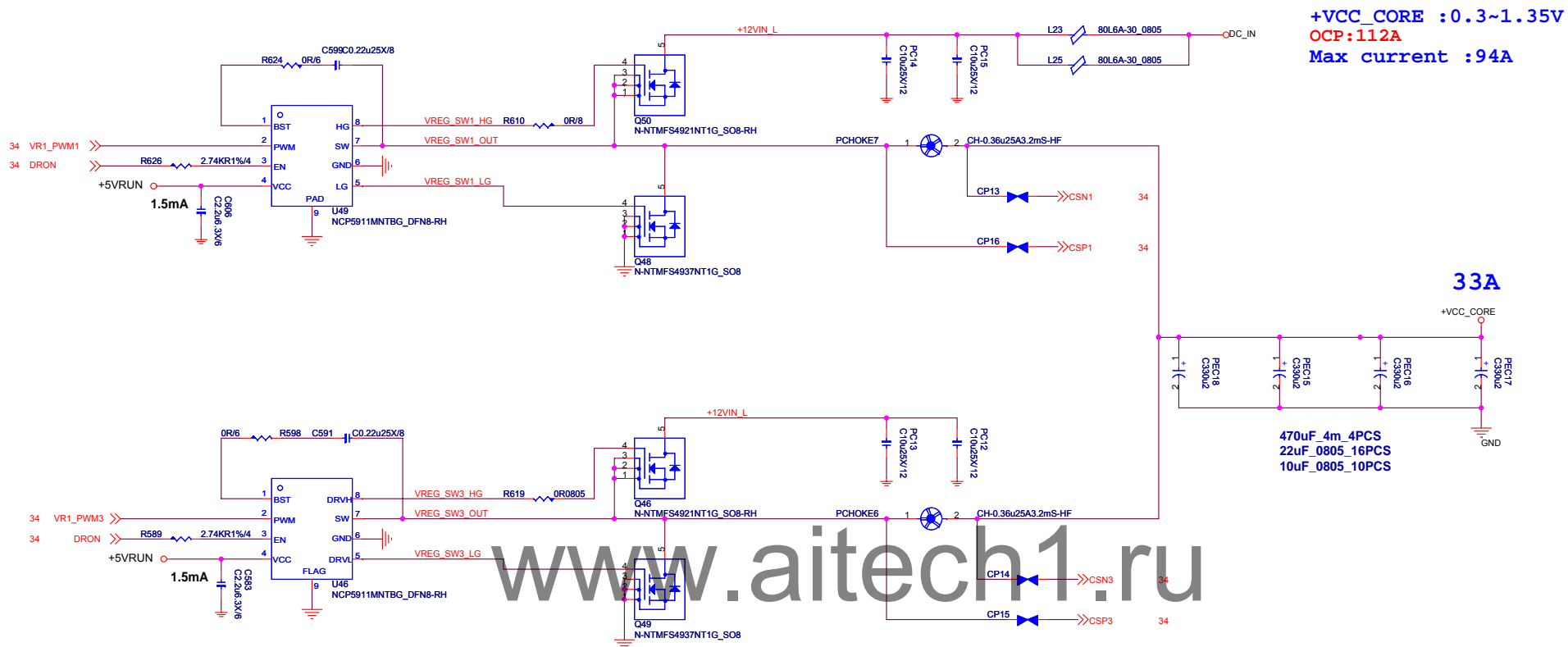
## Discharge SCH







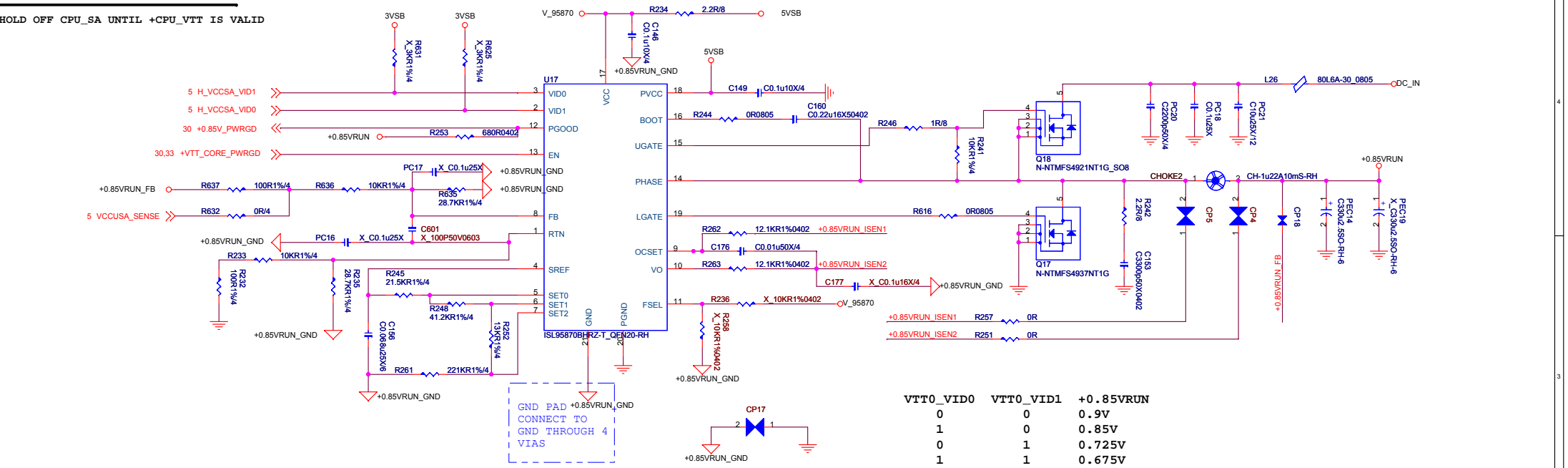




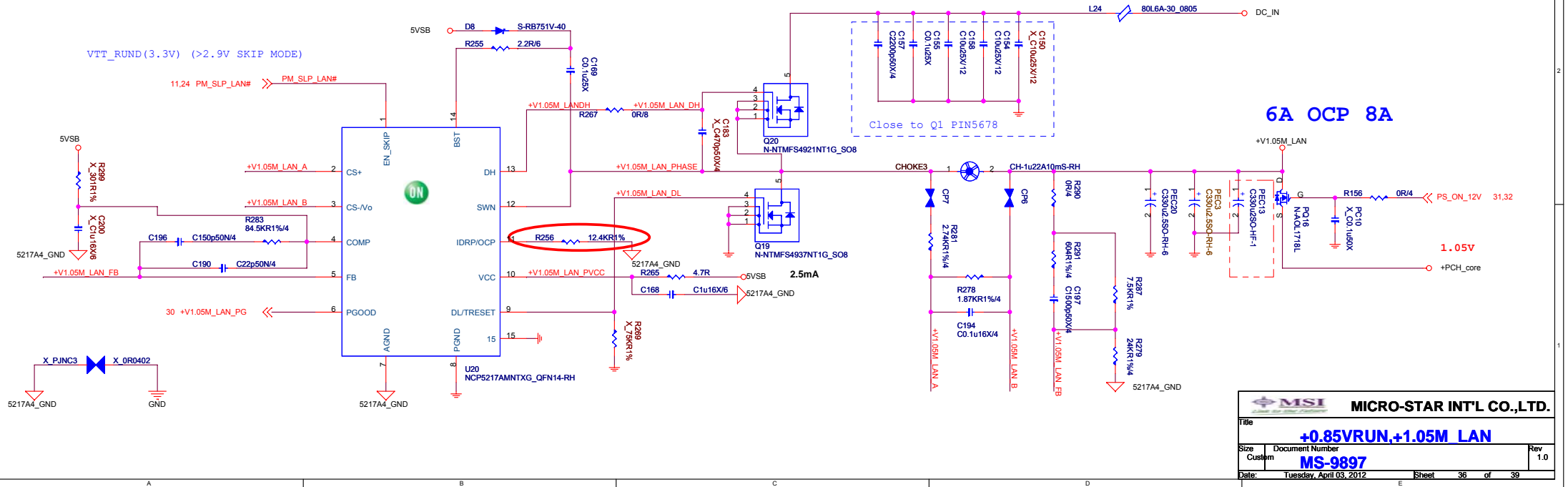
www.aitech1.ru

# CPU\_SA POWER(VCCSA)

HOLD OFF CPU\_SA UNTIL +CPU\_VTT IS VALID

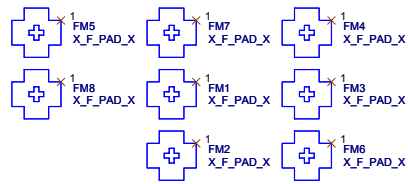


www.aitech1.ru

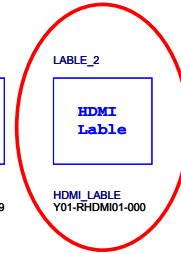
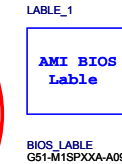
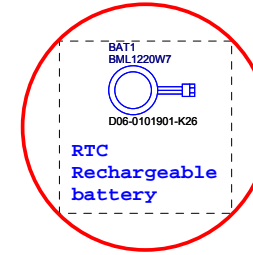
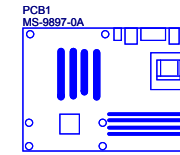
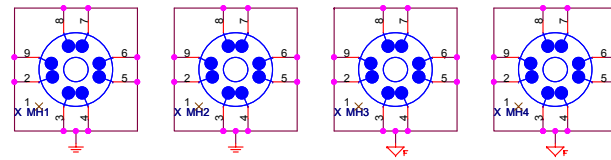




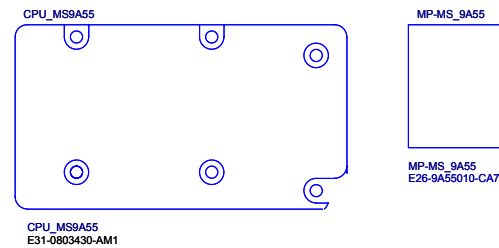
## Optical Fiducial Marks



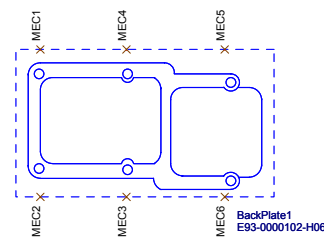
## Mounting Holes



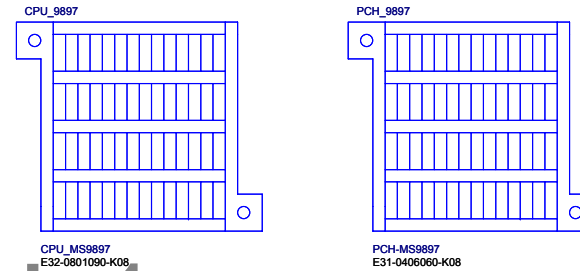
## For 9A55



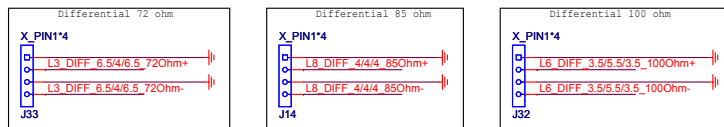
## For System and single Board



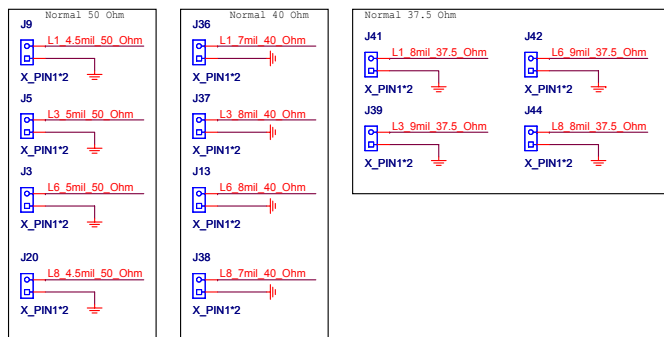
## For 9897



## Differential



## Single



www.aitech1.ru

- History 030317
- 1. Page-2 & Page-9\_Increase the processor debug capabilities(JTAG Function).
  - 2. Page-9\_D01-BA54C9-D07 of the new materials to replace the old material in the Circuit (location D7).
  - 3. Page-9\_The CON1 connector from the new name JRTC1.
  - 4. Page-9\_Add Part R271,R529
  - 5. Page-10\_Part R205,R201,RN6,R193,R163,RN7 Pull up to "3VSB".
  - 6. Page-10\_Parts R113, R112, R486, R487,replacement for 10KR 8P4R resistance "RN9".
  - 7. Page-10\_Parts R473, R472, R529, R539,replacement for 10KR 8P4R resistance "RN10".
  - 8. Page-11\_Part R555,R565,R567,R560 Pull up to "3VSB".
  - 9. Page-12\_DEL R202,R203
  - 10. Page-13\_Parts R568,R463,R559,R191 replacement for 10KR 8P4R resistance "RN11".
  - 11. Page-13\_Parts R569,R190,R563,R192,replacement for 10KR 8P4R resistance "RN12".
  - 12. Page-19\_Parts Q40,Q39 merged parts PQ18.
  - 13. Page-19\_Add Parts C654,C653 close to DVI Connect.
  - 14. Page-21\_Remove parts C128.
  - 15. Page-22\_The hardware circuit to increase the Com Port wake-up function at COM1 and COM2.
  - 16. Page-22\_Remove parts D11,R354.
  - 17. Page-22\_Part R359 Pull up to "+3VSUS".
  - 18. Page-24\_Network chip 82579LM pin 26 LEDO and the chip pin 27 LED1 swap.
  - 19. Page-24\_Remove parts C144,EC20,EC19,EC21,EC22,EC24,EC23,EC25,EC26.
  - 20. Page-24\_Part C134,C136,C148,C145 Pull up to "+3.3M LAN".
  - 21. Page-25\_Remove parts C181,EC28,EC27,EC29,EC30,EC32,EC31,EC33,EC34.
  - 22. Page-25\_Part C195,C192,C170,C174 Pull up to "+1.8VLAN2".
  - 23. Page-26\_Part R392,R660,R394,R366,R658,R381,C284,U36\_Pin5 Pull up to "3VSB".
  - 24. Page-26\_Remove parts R395,R377,R383,R382,R365,R364.
  - 25. Page-27\_Increase the Part FS7,FS8.
  - 26. Page-28\_Replacing the CPU and system fan connector,Pin1 and Pin3 swap(SYSFAN1,CPUFAN1).
  - 27. Page-28\_Remove parts R446.
  - 28. Page-31\_Standby state to generate 12 volts, fix the hardware circuit(Signal "PS\_ON #" must use signal "ATX\_PSON #" as a switch).
  - 29. Page-29\_Increase the sim card Circuit.
  - 30. Page-18\_The next version of the sound chip change for ALC886.
  - 31. Page-38\_Add HDMI symbol stickers.
  - 32. Page-38\_Replace the battery parts "D06-0101901-R26".
  - 33. Page-19\_Inductance value 0.12uH300mA replaced 0.082uH300mA in the circuit location L14, L15, L16.